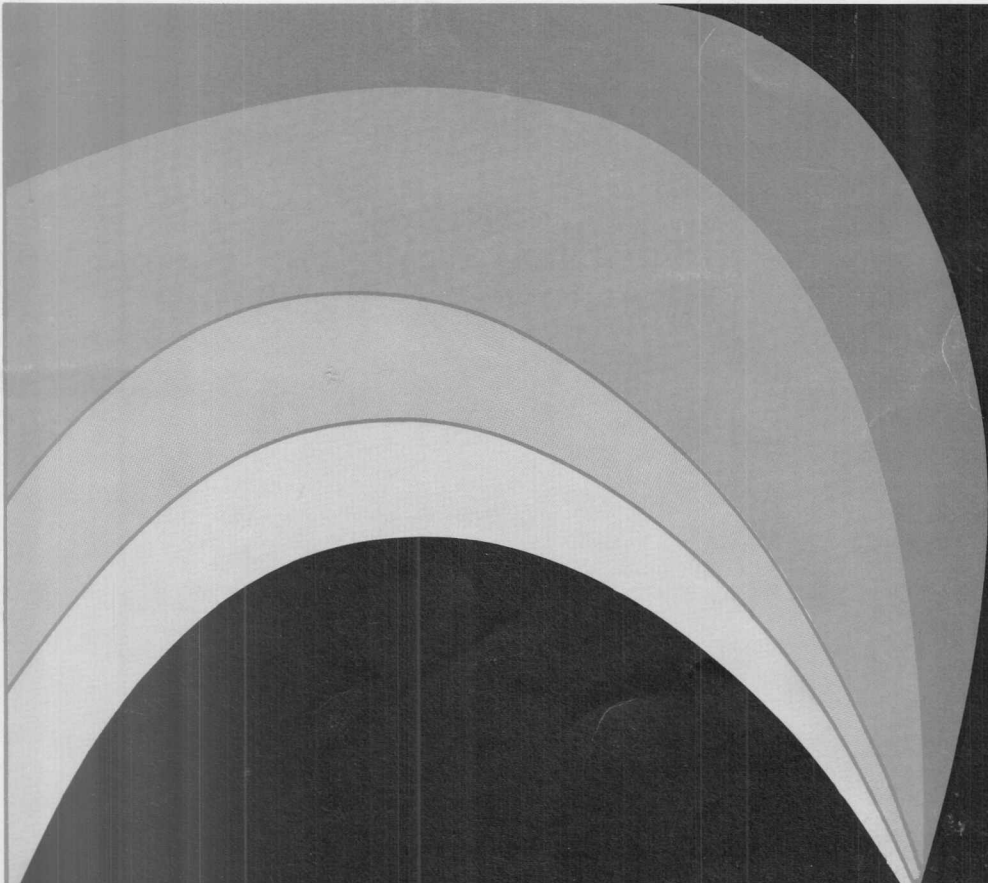


RCA Solid
State

COSMAC Microprocessor Product Guide

An abstract graphic consisting of several concentric, semi-circular arcs in shades of gray, creating a sense of depth and movement. The arcs are centered on the left side of the page and curve towards the right.

RCA 1800
MICROPROCESSORS

The RCA1800 microprocessor family includes all the elements you need to build an efficient microprocessor system.

Integrated Circuits (CDP1800 Series)

Our IC family boasts two important features: First, it's an all-CMOS family designed and manufactured by the First Family in CMOS. You get all the advantages of a CMOS system . . .

- minimal power-supply requirements
- completely static circuitry
- wide temperature range
- high noise immunity
- CMOS, TTL, NMOS compatibility . . .

plus the CMOS production expertise only RCA can offer.

Second, the CDP1800 series is comprehensive. It has a wide variety of ICs from which you can build your system . . .

- RAMs
- ROMs
- Input/Output (I/Os)
- Interfacing Circuits

Support Systems (CDP18S Series)

RCA's theme in developing its hardware and software has been "Graduated Steps to Microprocessing". In both functions and dollar investment, we offer discrete, logical steps for you to follow. Our approach is to help you progress from a learning state right on through to integral hardware/software system prototyping, covering each step with an appropriate tool . . .

- Microtutor
- COSMAC Evaluation Kit
- COSMAC Microterminal
- COSMAC Development System
- Floppy Disk
- Software Development Packages

All along the way, you'll use our manuals, application notes, and seminars to continually update your understanding of COSMAC.

CMOS technology, COSMAC architecture, and COSMAC support systems offer efficient, intelligent, economical programming and system design.

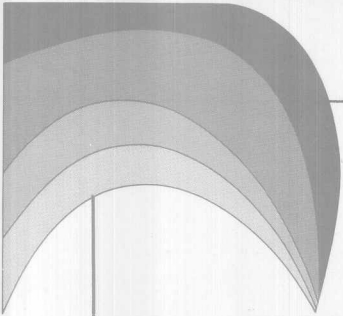
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1800 Family IC's and Support Systems

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The CDP1802 microprocessor is an 8-bit silicon-gate CMOS device for use as a general-purpose computing or control element.

Features:

- Standard 8-bit bidirectional data bus
- 16 X 16 matrix of registers for flexible programming
- DC to 6.4-MHz clock (single phase)
- Fast 2.5- or 3.75-us instruction time
- 91 basic instructions, 255 operation codes
- Minimal power-supply requirements — low current drain, single-supply, unregulated
- Split-power-supply option that allows for 10 V on internal parts of CPU and 5 V on interfacing lines
- On-chip, single-phase clock
- Memory addressing to 65K bytes
- Adaptability to any combination of standard RAM, ROM, or PROM memories
- Maskable interrupt and 4 testable external flag lines
- On-chip DMA controls
- Simple RESET, LOAD, PAUSE controls
- Programmable serial output (Q)

All CDP1800 Series ICs are available in two performance selections:

A type without a "C" suffix is the high-performance device. For example, the CDP1802 has:

- 3 V to 12 V recommended operating voltage range
- 2.5- or 3.75-us instruction time
- 40-mW power dissipation (typical)
- 6.4-MHz maximum clock input frequency at 10 V.

A type with a "C" suffix is the commercial device. For example, the CDP1802C has:

- 4 V to 6 V recommended operating voltage range
- 8 mW power dissipation (typical)
- 5- or 7.5-us instruction time
- 3.2-MHz maximum clock input frequency at 5 V

The Unique COSMAC Architecture

The COSMAC block diagram is shown at the top of the facing page. The principal feature of this system is a register matrix consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated or selected by the 14-bit binary code from one of the 4-bit designators P, X, or N. The contents of any register can be directed to any one of the following three paths:

1. to the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. to the accumulator (either of the two bytes can be gated to it);
3. to the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

How It Works

The registers in R can be used by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters — Any register can be used as the main program counter; the number of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction, the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the interrupt servicing routine. At all other times the register designated as program counter is at the discretion of the user.

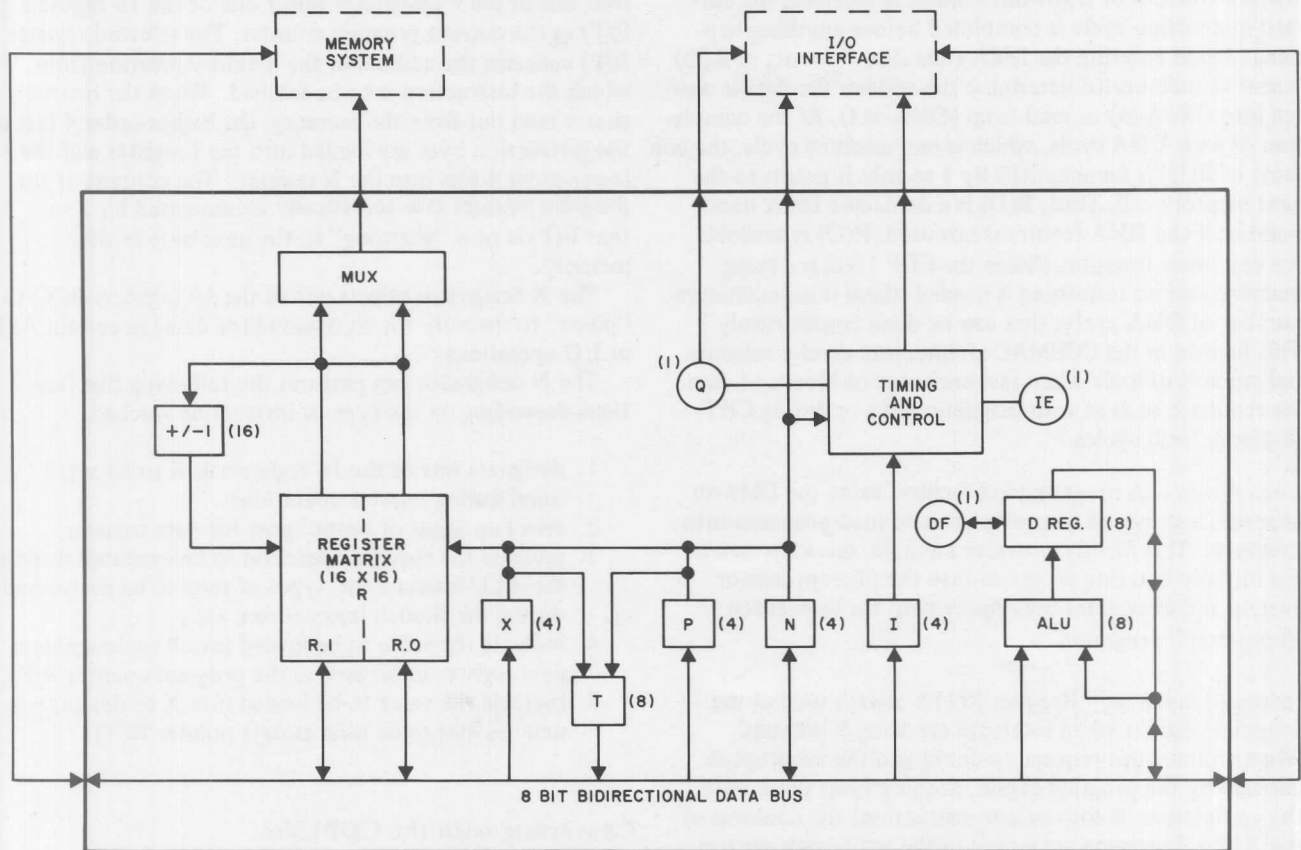
Data Pointers — The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see the Instruction Summary on pages 28–29):

1. ALU operations F0-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions — 70-73, 78.

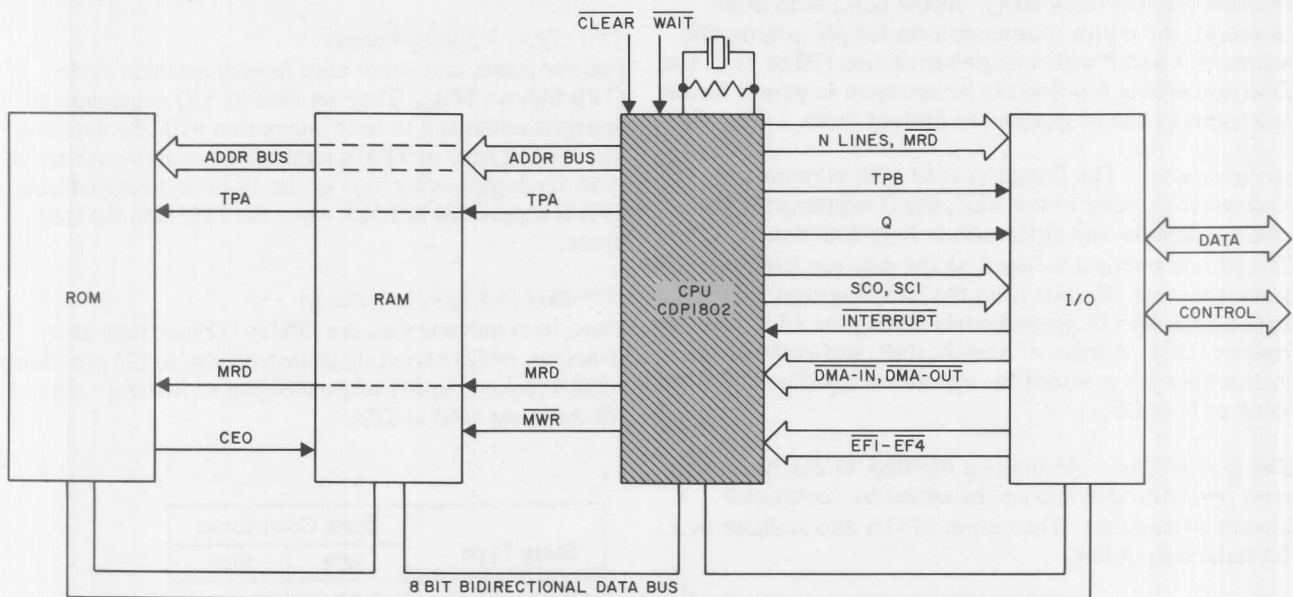
The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions (F8-FD, FF, 7C, 7D, 7F). During these instruction executions, the operation is referred to as "data immediate."

Data Registers — When registers in R are used to store bytes of data, four instructions are provided (AN, BN, 8N, 9N) which allow D to receive from or write into either the higher-order or lower-order byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

CDP1802 architecture



Typical CDP1802-based microcomputer system



DMA – Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-in or DMA-out request is received, the current instruction cycle is completed before anything happens. Upon entering the DMA state, the contents of R(O) is sent to memory to determine the address the data is written into (DMA-in) or read from (DMA-out). At the completion of each DMA cycle, which is one machine cycle, the contents of R(O) is incremented by 1 so that it points to the next memory cell. Thus, R(O) is a dedicated DMA data pointer; if the DMA feature is not used, R(O) is available for any other function. (Since the CDP 1802 is a static machine and no refreshing is needed, there is no maximum number of DMA cycles that can be done consecutively.) This feature in the COSMAC architecture saves a substantial amount of logic when fast exchange of blocks of data are required, such as with magnetic disks or during CRT-display-refresh cycles.

Load Mode – A program load facility, using the DMA-In channel, is provided to enable users to load programs into memory. This facility provides a simple, one-step means for initially entering programs into the microprocessor system and eliminates the requirement for specialized “bootstrap” programs.

Interrupt Servicing - Register R(1) is always used as the program counter when interrupt servicing is initiated. When an interrupt request comes in and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction) the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values: hex digit 2 in X and hex digit 1 in P. Interrupt enable is automatically deactivated to inhibit further interruptions. The user written interrupt routine is now in control; the contents of T are saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the return routine restores the pre-interrupted values of X and P with a single instruction (70 or 71). The interrupt-enable flip-flop can be activated to permit further interrupts or can be disabled to prevent them.

Accumulator – The D register is an 8-bit accumulator. Connected directly to the ALU, the D register provides one operand for any arithmetic or logic function. The second operand is found on the data bus from one of several sources. Results from the ALU's operation are then stored back into D, appropriately setting the 1-bit data flag register (DF). A series of branch, shift, and arithmetical instructions are provided for operations based on either the value of D or DF.

The Q Flip-Flop – An internal flip-flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a bit serial output line.

Instruction Cycles

COSMAC instructions consist of two machine cycles, a fetch cycle and an execute cycle (except for CN instruc-

tions, which require two execute cycles). Each machine cycle is 8 clock pulses long. During the fetch cycle, the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by 1 so that R(P) is now “pointing” to the next byte in the memory.

The X designator selects one of the 16 registers R(X) to “point” to memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. select an input or output port for data transfer;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, etc.,
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

Conversing with the CDP1802: Signal Descriptions

BUS 0 to BUS 7 (Data Bus)

8-bit bidirectional DATA BUS lines. These lines are used for transferring data among the memory, the microprocessor, and the I/O devices.

TPA, TPB (2 Timing Pulses)

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

SC0, SC1 (2 State Code Lines)

These lines indicate that the CPU is: (1) fetching an instruction, or (2) executing an instruction, or (3) processing a DMA request, or (4) acknowledging an interrupt request. All states are valid at TPA.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

HIGH = V_{CC}
LOW = V_{SS}

MWR (Write Pulse)

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

MRD (Read Level)

A low level (V_{SS}) on MRD indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, MRD is useful for driving memory bus separators. It is also used to indicate the direction of data transfer during an I/O instruction:

MRD= V_{CC} : Data from I/O to CPU and Memory

MRD= V_{SS} : Data from Memory to I/O

MA0 to MA7 (8 Memory Address Lines)

The higher-order byte of a 16-bit COSMAC memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system are strobed into external address latches by timing pulse TPA. (The CDP1831 and CDP1833 ROM's have built-in-address latches as well as other system-simplifying features, as listed on page 11.) The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 65K bytes.

N0, N1, N2 (I/O Command)

These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding three lower order bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 and is indicated by the level of the MRD signal.

INTERRUPT, DMA-IN, DMA-OUT (3 I/O Requests)

These signals are sampled by the CDP1802 during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed.

DMA Action: Finish executing current instruction; R(O) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(O).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority, followed by DMA-OUT and then INTERRUPT.

EF1 to EF4 (4 Flags)

These lines enable the I/O controllers to transfer status information to the processor. The lines can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which

case the program must routinely test the status of these flags. The flags are sampled at the beginning of every S1 cycle.

Q Flip-Flop

Single-bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK

Input for externally generated single-phase clock. The maximum clock frequency is 6.4 MHz at $V_{CC} = V_{DD} = 10$ volts. The clock is counted down internally to 8 clock pulses per machine cycle.

XTAL

Connection to be used with clock input terminal for an external crystal if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and XTAL) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39.

WAIT, CLEAR (2 Control Lines)

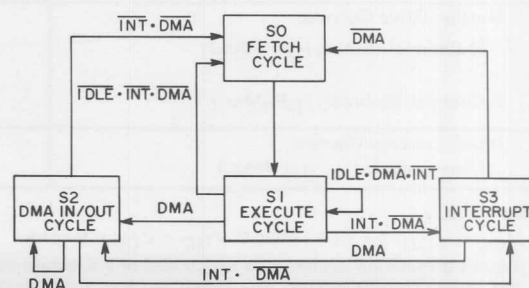
Provide four control modes as listed in the following truth table:

<u>CLEAR</u>	<u>WAIT</u>	MODE
H	H	RUN
H	L	PAUSE
L	H	RESET
L	L	LOAD

The functions of the modes are defined as follows:

Run — May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

The CDP1802 state transitions when in the RUN mode are shown below. Each machine cycle requires the same period of time — 8 clock pulses. The execution of an instruction pulse requires either two or three machine cycle, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response.



OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$ Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES		UNITS
	V_{CC}^1 (V)	V_{DD} (V)	CDP1802D	CDP1802CD	
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	—	—	3 to 12	4 to 6	V
Recommended Input Voltage Range	—	—	V_{SS} to V_{CC}	V_{SS} to V_{CC}	V
Clock Input Rise or Fall Time, t_r or t_f	3-15	3-15	5	5	μs
Instruction Time ²	5	5	5	5	μs
	5	10	3.2	—	
	10	10	2.5	—	
DMA Transfer Rate	5	5	400	400	Kb/s
	5	10	625	—	
	10	10	800	—	
Clock Input Frequency, f_{CL}	5	5	DC - 3.2	DC - 3.2	MHz
	5	10	DC - 5.0	—	
	10	10	DC - 6.4	—	
Clock Pulse Width, t_{WL} , t_{WH}	5	5	160	160	ns
	5	10	100	—	
	10	10	80	—	
Clear Pulse Width	5	5	300	300	ns
	5	10	200	—	
	10	10	150	—	

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

CHARACTERISTIC	CONDITIONS		CDP1802D VALUES	CDP1802CD VALUES	UNITS
	V_O (V)	V_{CC}, V_{DD} (V)			
Quiescent Device Current, I_L (Max.)	—	5, 5	100	500	μA
	—	10, 10	500	—	
	—	15, 15	1000	—	
Total Power Dissipation: OP CODE "00" (Typ.) $f = \text{MHz}$	3.2	5, 5	6	8	mW
	5.0	5, 10	30	—	
	6.4	10, 10	40	—	
Output Voltage: Low-Level, V_{OL} (Max.) High-Level, V_{OH} (Min.)	—	5, 5	0.05	0.05	V
	—	10, 10	0.05	—	
	—	5, 5	4.5	4.5	
	—	10, 10	9.5	—	
Noise Immunity: Inputs Low, V_{NL} (Min.) Inputs High, V_{NH} (Min.)	0.5	5, 5	1.5	1.5	V
	1	10, 10	3	—	
	4.5	5, 5	3.5	3.5	
	9	10, 10	3.45	—	
Output Drive Current: N-Channel (Sink), I_{DN} (Min.) P-Channel (Source), I_{DP} (Min.)	0.4	5, 5	1.8	1.8	mA
	0.5	10, 10	3	—	
	2.5	5, 5	-0.3	-0.3	
	9.5	10, 10	-0.8	—	
Input Leakage Current (Any Input), I_{IL} , I_{IH} (Max.)	—	5, 5	± 1	± 1	μA
	—	15, 15	± 1	—	

Notes:

- $V_{CC} \leq V_{DD}$; for CDP1802CD $V_{DD} = V_{CC} = 5$ volts.
- Equals 2 machine cycles—one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles—one Fetch and two Execute operations.

Pause — Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

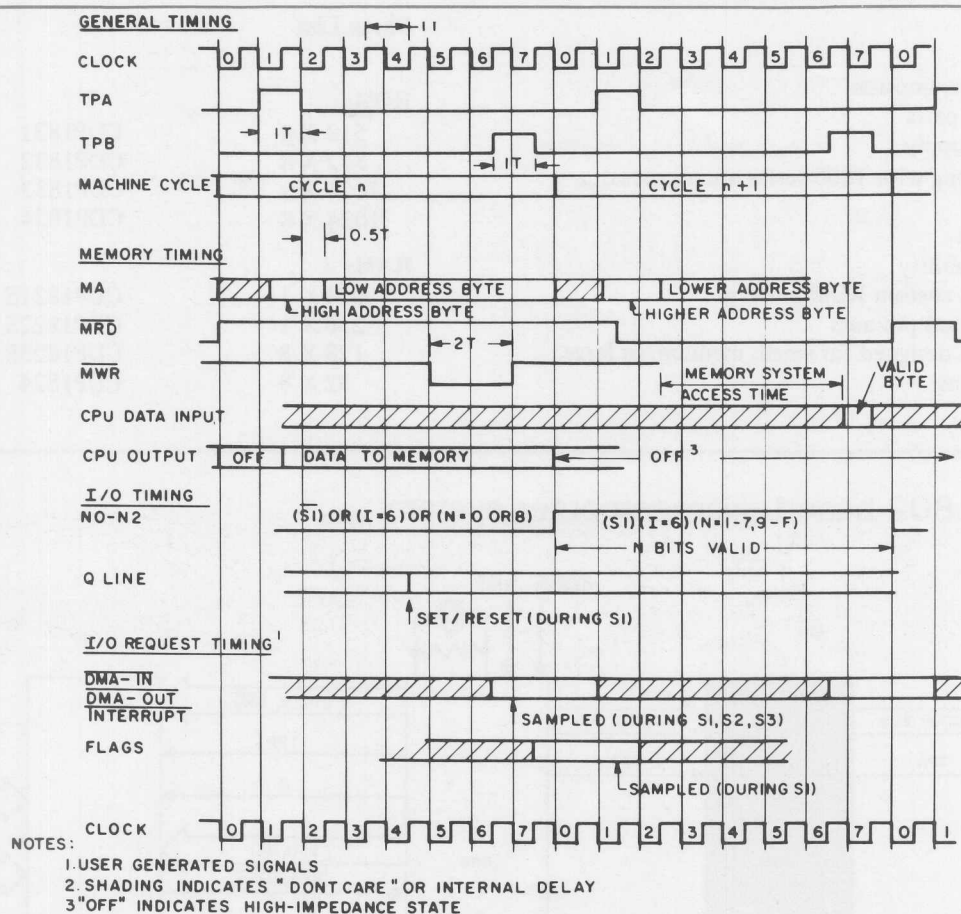
Reset — Registers I, N, Q are reset, IE is set, and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle. During this cycle the CPU remains in S1 and registers X, P, and R(O) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle. The next cycle is an S0, S1, or S2, but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE so as to preclude interrupts until ready for them.

Power-up reset can be realized by connecting an external RC to **CLEAR**.

Load — Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

V_{DD} , V_{SS} , V_{CC} (Power Levels)

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at high speed while interfacing with various external circuit technologies, including TTL at 5 volts. V_{CC} must be less than or equal to V_{DD} . All outputs swing from V_{SS} to V_{CC} . The recommended input voltage swing is V_{SS} to V_{CC} .



CDP1802 Timing Diagram

CDP1802 INSTRUCTION EXECUTION TIMES

1-Byte instructions require 2 Machine Cycles: 1 Fetch, 1 Execute.

2-Byte instructions also require 2 Machine Cycles: 1 Fetch, 1 Execute.

3-Byte instructions require 3 Machine Cycles: 1 Fetch, 2 Executes.

INSTRUCTION SIZE			% OF TOTAL REPERTOIRE	INSTRUCTION TIME @ f =		
Bytes of Op. Code	Bytes of Address or Data	Total Bytes of Memory		6.4 MHz	3.2 MHz	2 MHz
1	0	1	93	2.5 μ s	5 μ s	8 μ s
1	1	2	7	3.75 μ s	7.5 μ s	12.1 μ s
1	2	3	—	2.6 μ s	5.2 μ s	8.3 μ s
Average Instruction Execution Time			—	2.6 μ s	5.2 μ s	8.3 μ s

Memory Support Circuits for the CDP1802 microprocessor include both CMOS ROMs and RAMs with many system-simplifying capabilities.

Features:

- Low power consumption
- All fully static parts
- Single power supply
- Direct interfacing with 1800-series microprocessor systems
- 3-state outputs
- TTL drive capability
- Small MOQ on custom ROM patterns
- Industry standard pin-outs
- Different parts designed for small, medium, or large memory systems

Parts List

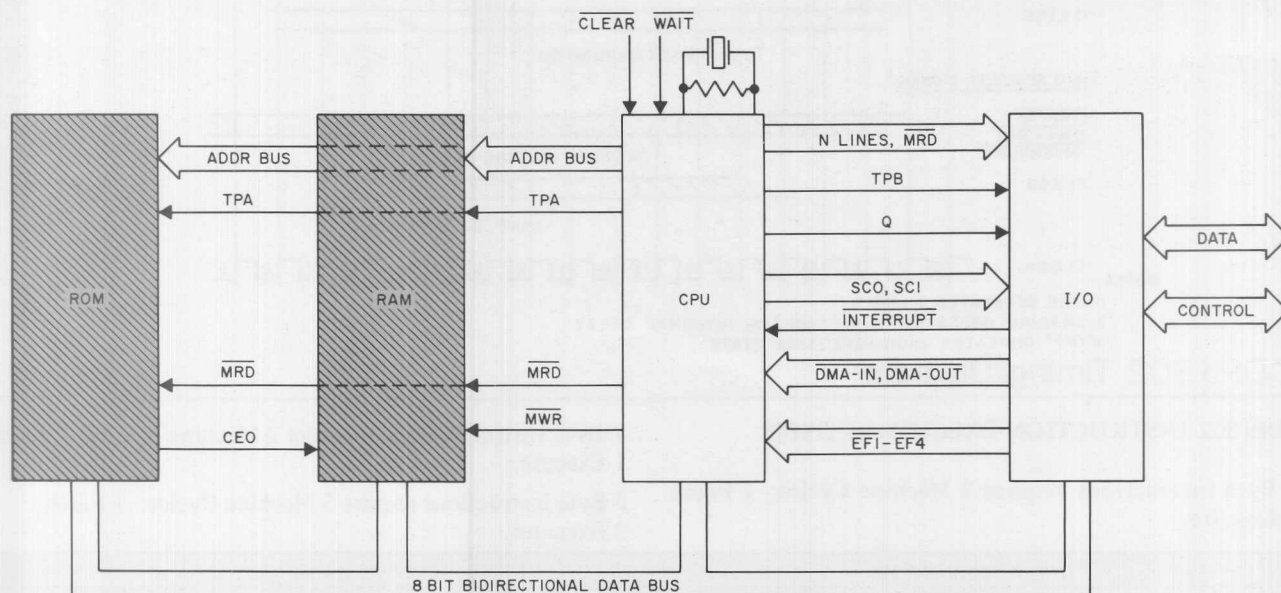
ROMs

512 X 8	CDP1831
512 X 8	CDP1832
1024 X 8	CDP1833
1024 X 8	CDP1834

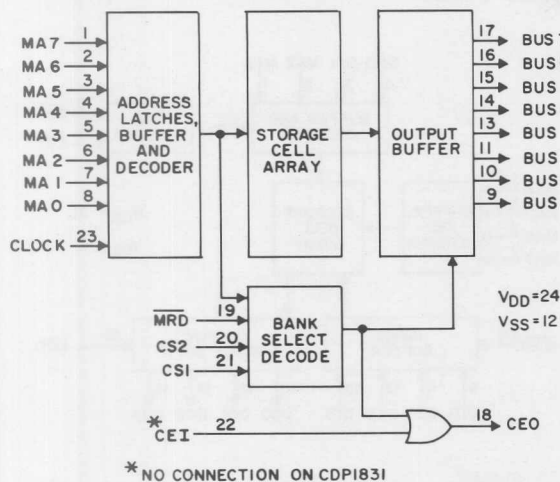
RAMs

1024 X 1	CDP1821S
256 X 1	CDP1822S
128 X 8	CDP1823S
32 X 8	CDP1824

Typical CDP1802-based microcomputer system



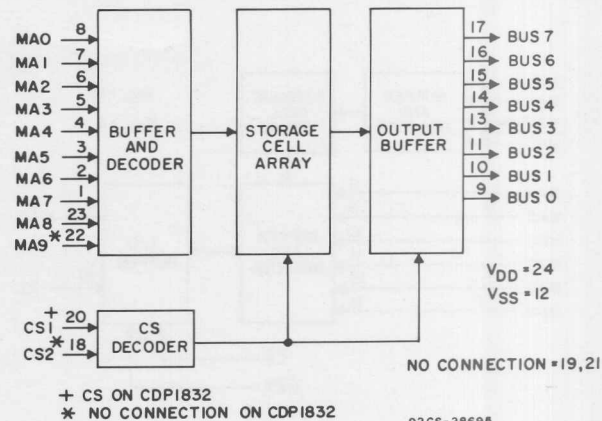
CDP1831 512x8 ROM



- User programs ROM's location in memory field
- On-chip latch for higher-order memory address
- CEO signal indicates status of chip (selected or not)
- Can minimize or eliminate memory decoding logic
- Either 512 or 1024 bytes of ROM in same pin-out
- 3 chip selects
- 3-state outputs
- Single power supply
- Industry standard 24-pin packages
- 400-ns access time at 10 V
- Directly compatible with CDP1802

92CS-28694

CDP1832 512x8 ROM



- CDP1832 is a direct replacement for the 2704 PROM
- CDP1834 is a direct replacement for the 2708 PROM
- Directly compatible with the CDP1802
- Single power supply
- 400-ns access time at 10 V
- 3-state outputs
- Industry standard 24-pin packages
- Accepts standard memory address decoding

92CS-28695

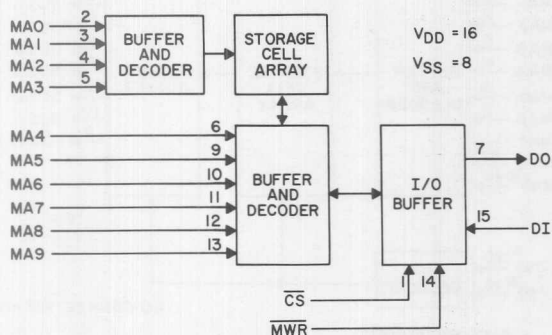
CDP1834 1024x8 ROM

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES								UNITS
	V _O (V)	V _{DD} (V)	CDP-1831D	CDP-1831CD	CDP-1832D	CDP-1832CD	CDP-1833D	CDP-1833CD	CDP-1834D	CDP-1834CD	
Static											
Quiescent Device Current, I _L (Max.)	— — —	5 10 15	100 500 1000	1000 — —	100 500 1000	1000 — —	100 500 1000	1000 — —	100 500 1000	1000 — —	μA
Output Drive Current:											
N-Channel (Sink), I _{DN} (Min.)	0.4 0.5	5 10	0.4 0.9	0.4 —	0.4 0.9	0.4 —	3.2 7.2	3.2 —	3.2 7.2	3.2 —	mA
P-Channel (Source), I _{DP} (Min.)	4.6 9.5	5 10	-0.25 -0.5	-0.25 —	-0.25 -0.5	-0.25 —	-2 -5	-2 —	-2 -5	-3.2 —	
Dynamic: t _r ,t _f =10 ns, C _L =50 pF (Typical Values)											
Access Time From Address Change, t _{AA}	— —	5 10	850 400	850 —	850 400	850 —	850 350	850 —	850 350	850 —	ns
Access Time From Chip Select, t _{ACS}		5 10	— —	— —	400 200	400 —	700 300	700 —	700 300	700 —	ns
Chip Enable Output Delay Time From CS, t _{CO}	— —	5 10	400 200	400 —	— —	— —	400 200	400 —	— —	— —	ns

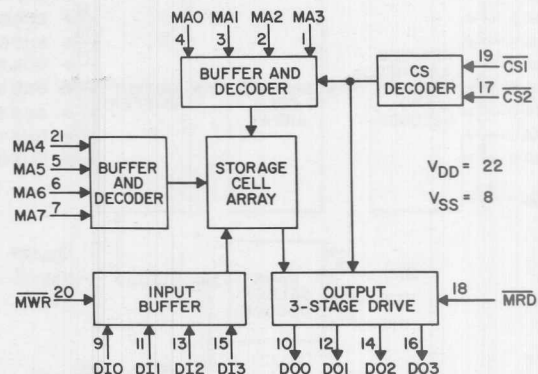
Note: Dynamic power dissipation is pattern dependent.

CDP1821S 1024x1 RAM



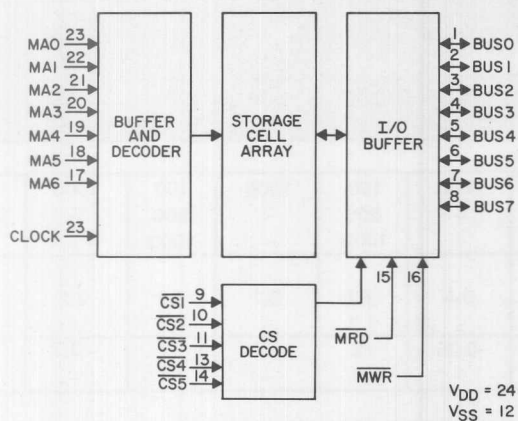
- Directly interfaces with CDP1802
- Good for large RAM memory systems
- Single power supply
- Industry standard 16-pin packages for high board density
- 200-ns access time at 10 V
- CS can be used as an additional address line — no clocking required
- Standby power consumption of 15 mW (typ.) at 10 V

CDP1822S 256x4 RAM



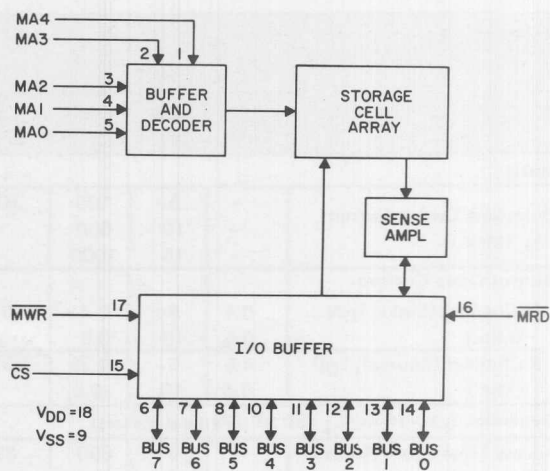
- 2 chip selects for easy memory expansion
- 200-ns access time at 10 V
- Output disable permits common I/O systems
- Industry standard 22-pin packages
- Standby power consumption of 15 mW (typ.) at 10 V

CDP1823S 128x8 RAM



- 3-state bus
- Directly interfaces with CPUs
- Standby power consumption of 15 mW (typ.) at 10 V
- Single power supply
- 200-ns access time at 10 V
- Industry standard 24-pin packages
- Designed for medium-sized RAM requirements

CDP1824 32x8 RAM



- 300-ns access time at 10 V
- Fully decoded and static
- Separate read and write signals
- Standby power consumption of 5 mW (typ.) at 10 V
- Low quiescent and operating power
- Excellent for minimum RAM systems (e.g., stacks)
- Industry standard 18-pin packages
- CS for memory expansion

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUES										UNITS
		V _O (V)	V _{DD} (V)	CDP- 1821SD	CDP- 1821SCD	CDP- 1822SD	CDP- 1822SCD	CDP- 1823SD	CDP- 1823SCD	CDP- 1824D	CDP- 1824CD	
Static (Maximum Values)												
Quiescent Device Current, I _L (max.)		— —	5 10	300 1500	1500 —	300 1500	1500 —	300 1000	1500 —	100 500	500 —	μA
Total Power-Dissipation, P _D at 1 μs cycle		— —	5 10	5 20	8 —	8 35	10 —	15 65	20 —	10 50	12 —	mW
Output Voltage: Low-Level, V _{OL}		—	5–10	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	V
High-Level, V _{OH}		— —	5 10	4.99 9.99	4.99 —	4.99 4.99	4.99 —	4.99 9.99	4.99 —	4.99 4.99	4.99 —	
Noise Margin: V _{NML}	Any Input	0.5 1	5 10	1 1.5	1 —	1 1.5	1 —	1 1.5	1 —	1 1.5	1 1.5	V
V _{NMH}	Any Input	4.5 9	5 10	1 1.5	1 —	1 1.5	1 —	1 1.5	1 —	1 1.5	1 1.5	
Input Leakage, I _{IL} , I _{IH}	Any Input	—	5–10	±1	±1	±1	±1	±1	±1	±1	±1	μA
Data Bus Leakage	Output Disabled or Chip Not Selected	—	5–10	±5	±5	±5	±5	±5	±5	±1	±1	μA
Output Drive Current: N-Channel (Sink), I _{DN} (Min.)	Any Output	0.4 0.5	5 10	2.5 3.5	2.5 —	.4 1.8	.4 —	1.2 1.8	1.2 —	2.2 4.2	2.2 —	mA
P-Channel (Source), I _{DP} (Min.)	Any Output	4.6 9.5	5 10	–1.25 –1.5	–1.25 —	.4 –1.8	.4 —	–0.8 –1.8	–0.8 —	–1.1 7.2	–1.1 —	
Dynamic: t _r , t _f = 10 ns, C _L = 50 pF												
Read Operation												
Access Time From Address Change, t _{AA}		— —	5 10	350 200	350 —	350 200	350 —	350 200	350 —	600 300	600 300	ns
Access Time From Chip Select, t _{AC}		— —	5 10	260 160	260 —	260 160	260 —	250 150	250 —	600 300	600 —	ns
Output Active From MRD, t _{AM}		— —	5 10	— —	— —	250 150	250 —	250 150	250 —	600 300	600 —	ns
Write Operation												
Write Pulse Width, t _{WW}		— —	5 10	150 100	150 —	150 100	150 —	150 100	150 —	350 150	350 —	ns
Data Setup Time, t _{DS}		— —	5 10	150 100	150 —	150 100	150 —	150 100	150 —	350 150	350 —	ns
Data Hold Time, t _{DH}		— —	5 10	70 35	70 —	70 35	70 —	100 50	100 —	60 30	60 —	ns
Chip Select Setup Time, t _{CS}		— —	5 10	250 110	250 —	250 110	250 —	250 150	250 —	500 350	500 —	ns
Address Setup Time, t _{AS}		— —	5 10	190 130	190 —	190 130	190 —	200 150	200 —	500 350	500 —	ns
Address Hold Time, t _{AH}		— —	5 10	110 70	110 —	110 70	110 —	100 50	100 —	100 50	100 —	ns
Capacitance												
Input/Output, C _{BUS} :												
Input, C _I		—		5	5	5	5	15	15	5	5	pF
Output, C _O		—	—	5	5	5	5	5	5	—	—	pF

Input/Output Support Circuits for the CDP1802 microprocessor make use of many signals to optimize cost and performance.

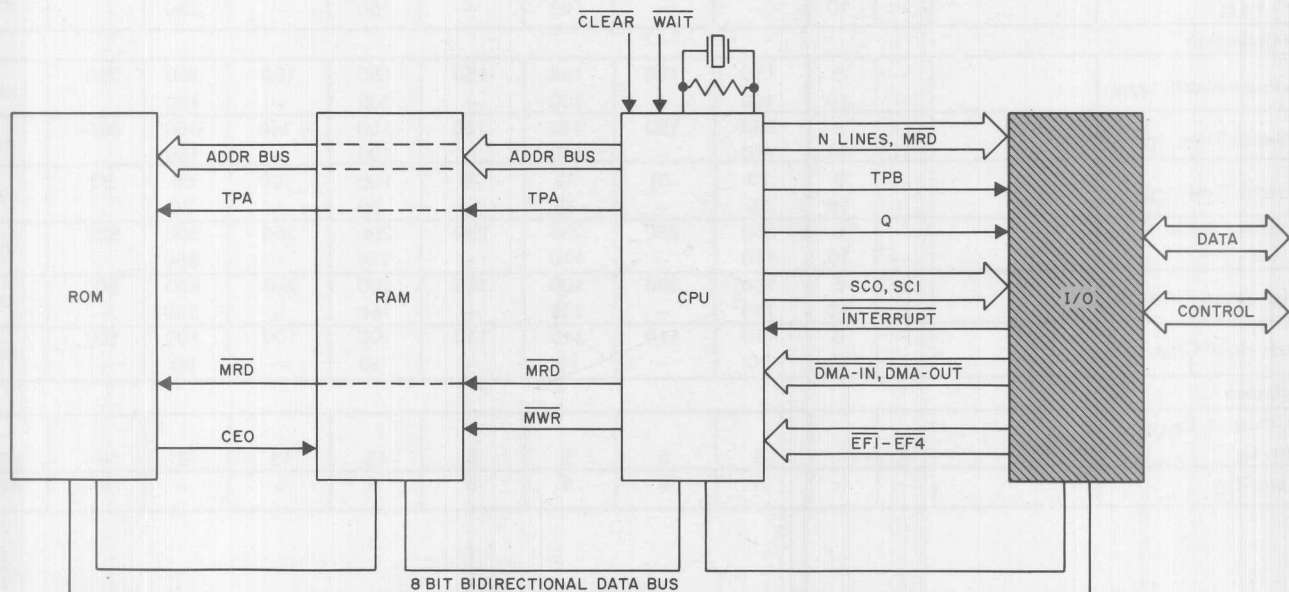
Features:

- 4 CPU-tested flag inputs (EF) for slowly varying binary inputs or for I/O-to-CPU signalling
- Interrupt request; maskable for flexibility
- 2 DMA request lines, In and Out, with Memory pointer and control logic on the CDP1802
- 2 state-code output lines to tell I/O devices what the CPU is doing
- Programmable output bit Q
- 3 I/O command lines (N) for programmed control of memory-I/O transfer
- Memory data strobe (TPB) for clean and easy capture of data by I/O device

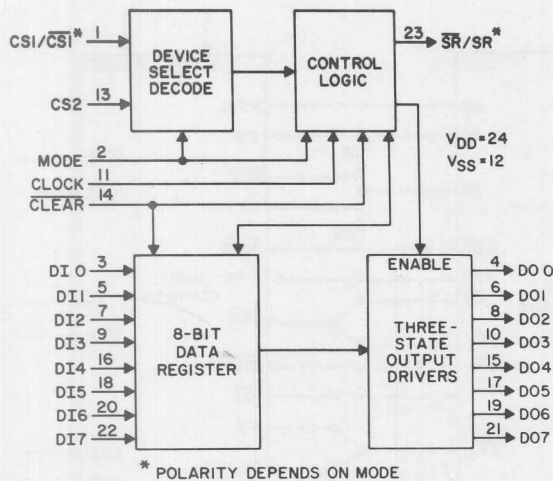
Parts List

I/O Port	CDP1852
N-Bit Decoder	CDP1853
UART (Universal Asynchronous Receiver/Transmitter)	CDP1854
4-Bit Bus Buffer/Separator (Memory)	CDP1856
4-Bit Bus Buffer/Separator (I/O)	CDP1857
Memory-Address Latch with 1 of 4 Decoder	CDP1858
Memory-Address Latch with Dual 1 of 4 Decoders	CDP1859

Typical CDP1802-based microcomputer system

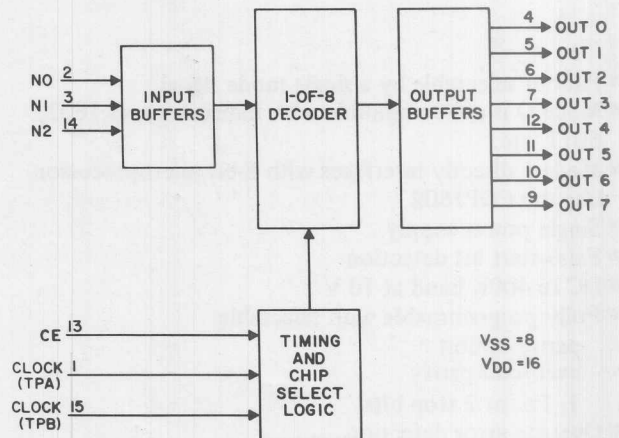


CDP1852 8-Bit I/O Port



- 8-bit data latch
- Directly interfaces with CPU
- Industry standard 24-pin packages
- 3-state outputs
- Clear input
- Designed for use in 8-bit microprocessor systems
- Fully static
- Mode selectable

CDP1853 N-Bit Decoder



- Allows easy expansion of I/O systems
- Buffered inputs and outputs
- Functions at full microprocessor speed
- Ties directly to "N" lines on CDP1802
- Strobed outputs for spike-free decoding
- Low power dissipation
- Provides control of up to 14 I/O devices

ELECTRICAL CHARACTERISTICS at TA = 25°C

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES		UNITS
	V _O (V)	V _{DD} (V)	CDP-1852D	CDP-1852CD	
Static (Maximum Values)					
Quiescent Device Current, I _L	—	5	50	100	μA
	—	10	100	—	
	—	15	500	—	
Input Leakage, I _{IL} , I _{IH}	Any Input	5-10	±1	±1	μA
Data Bus Leakage		5-10	±1	±1	μA
Output Drive Current:					
N-Channel (Sink), I _{DN} (Min.)	0.4	5	1.6	1.6	mA
	0.5	10	3.6	—	
P-Channel (Source), I _{DP} (Min.)	4.6	5	-1.6	-1.6	
	9.5	10	-3.6	—	
Dynamic: t _r ,t _f =10 ns, C _L =50 pF (Typical Values)					
Propagation Delay Times:					
Output from CS, t _{CA}	—	5	200	200	ns
	—	10	100	—	
Data to Output, t _{OD}	—	5	200	200	
	—	10	100	—	
Capacitance, C _I , C _O	—		5	5	pF

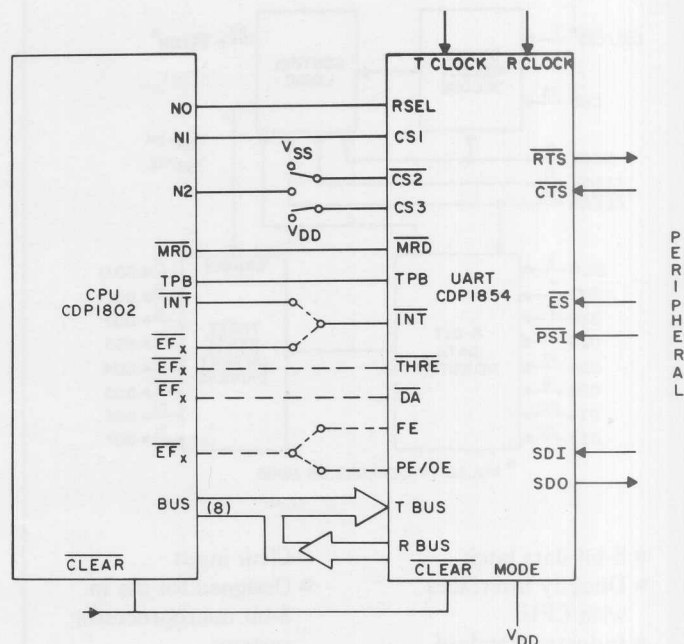
ELECTRICAL CHARACTERISTICS at TA = 25°C

CHARACTERISTIC	TEST CONDITIONS			TYPICAL VALUES		UNITS
		V _O (V)	V _{DD} (V)	CDP- 1853D	CDP- 1853CD	
Static						
Quiescent Device Current, I _L (max.)		— — —	5 10 15	50 100 500	100 — —	μA
Output Voltage: Low-Level, V _{OL} High-Level, V _{OH}		— — —	5-10 5 10	0.01 4.99 9.99	0.01 4.99 —	V
Noise Margin: V _{NML} V _{NMH}	Any Input Any Input	0.5 1 4.5 9	5 10 5 10	1 1.5 1 1.5	1 — 1 —	V
Output Drive Current: N-Channel (Sink), I _{DN} (min.) P-Channel (Source), I _{DP} (min.)	Any Output Any Output	0.4 0.5 4.6 9.5	5 10 5 10	1.6 3.6 -1.6 -3.6	1.6 — -1.6 —	mA —
Input Leakage, I _{IL} , I _{IH}	Any Input	—	5-10	±1	±1	μA

CDP1854

UART

- Pin-out selectable by a single mode signal
- Mode 0 is pin-compatible with industry types 1602, 6011, etc.
- Mode 1 directly interfaces with 8-bit microprocessor like the CDP1802
- Single power supply
- False-start bit detection
- DC to 400K baud at 10 V
- Fully programmable with selectable:
 - parity inhibit
 - even/odd parity
 - 1, 1½, or 2 stop bits
- Overrun error detection
- External word length selection—5, 6, 7, or 8 bits
- Full or half duplex operation
- Full temperature range operation
- Low power dissipation—5 mW typ. at 10 V
- Standard 40-pin packages

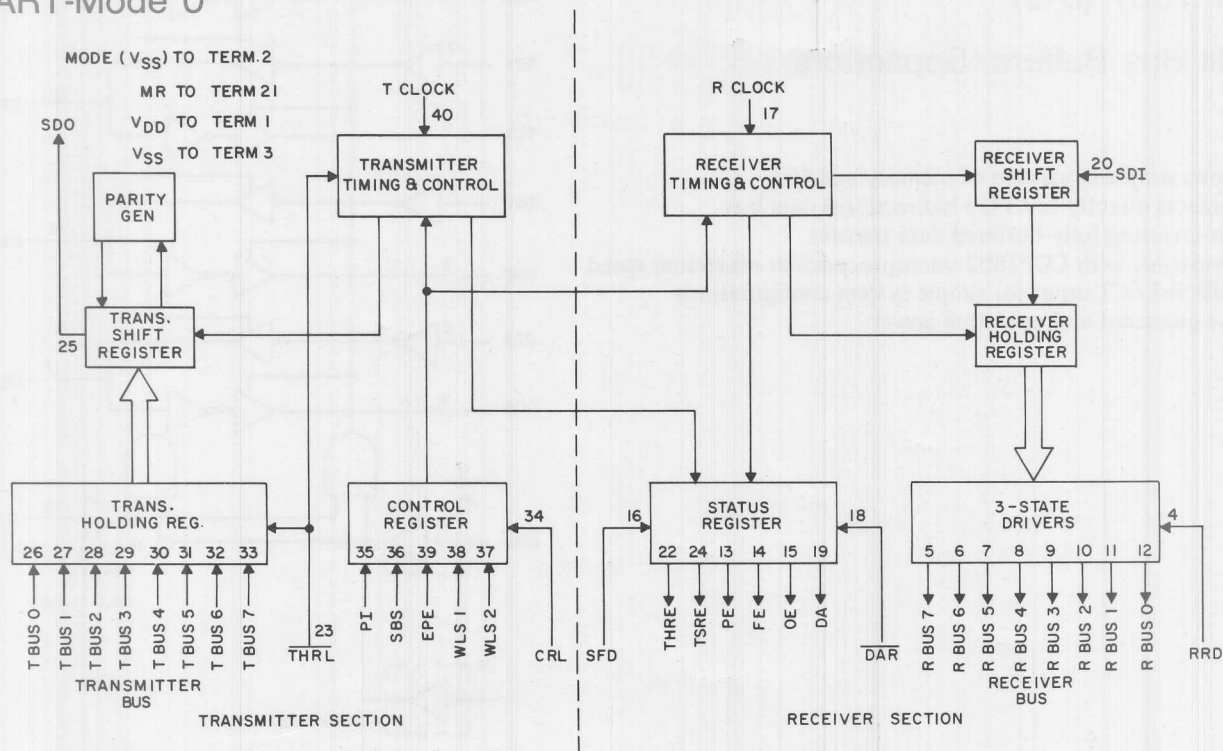


ELECTRICAL CHARACTERISTICS at TA = 25°C

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES		UNITS
	V _O (V)	V _{DD} (V)	CDP1854D	CDP1854CD	
Static					
Quiescent Device Current, I _L	—	5	100	500	μA
	—	10	500	—	
	—	15	1000	—	
Output Voltage: Low-Level, V _{OL}	—	5	0.01	0.01	V
	—	10	0.01	—	
High-Level, V _{OH}	—	5	5	5	V
	—	10	10	—	
Noise Immunity: Inputs Low, V _{NL}	0.5	5	2.25	2.25	V
	1	10	3.45	—	
Inputs High, V _{NH}	4.5	5	2.25	2.25	V
	9	10	3.45	—	
Output Drive Current: N-Channel (Sink), I _{DN}	0.4	5	0.4	0.4	mA
	0.5	10	0.9	—	
P-Channel (Source), I _{DP}	2.5	5	-1.6	-1.6	
	4.6	5	-0.4	-0.4	
	9.5	10	-1	—	
	—	—	—	—	
Input Leakage Current (Any Input), I _{IL} , I _{IH}	—	5	±1	±1	μA
	—	10	±1	—	
Dynamic, C _L = 50 pF					
Status Flag Disconnect to- STATUS OUT Delay, t _{SS}		5	200	200	ns
		10	100	—	
Receiver Register Disconnect to- DATA OUT Delay, t _{RDB}		5	200	200	ns
		10	100	—	
Total Power Dissipation, P _D at 3.2 MHz		5	5	7	mW
		10	15	—	

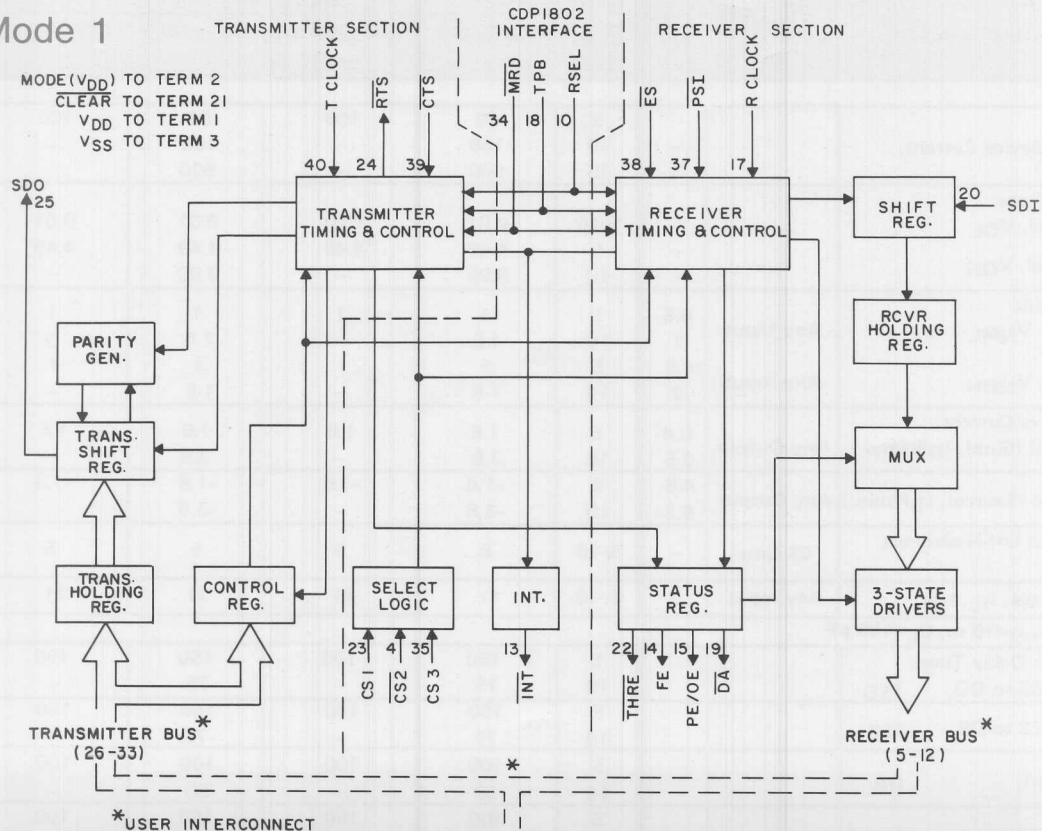
CDP1854

UART-Mode 0



CDP1854

UART-Mode 1

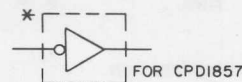
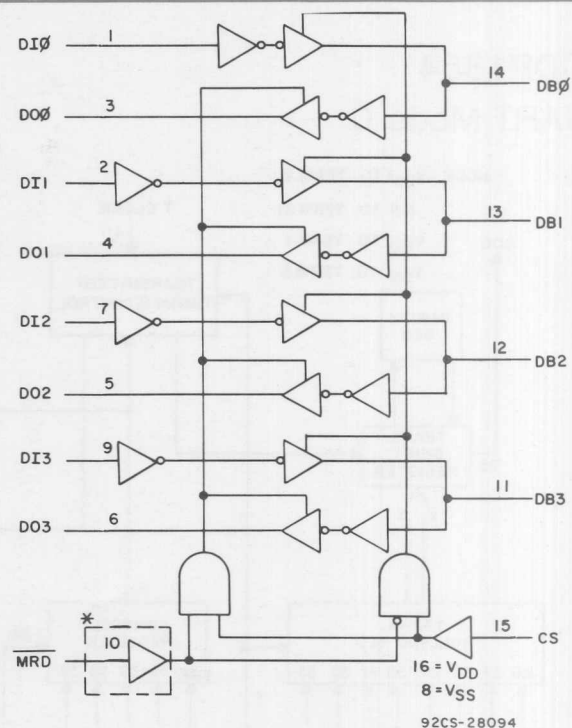


CDP1856 (Memory)

CDP1857 (I/O)

4-Bit Bus Buffers/Separators

- Allows simple expansion of memory and I/O
- Connects directly to CPU's bidirectional data bus
- Non-inverting fully buffered data transfer
- Compatible with CDP1802 microprocessor at maximum speed
- CHIP SELECT input for simple system configurations
- Low quiescent and operating power

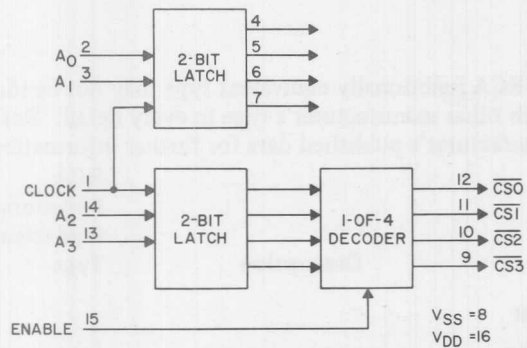


ELECTRICAL CHARACTERISTICS at TA = 25°C

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES				UNITS	
	V _O (V)	V _{DD} (V)	CDP1856D	CDP1856CD	CDP1857D	CDP1857CD		
Static								
Quiescent Device Current, I _L (max.)		—	5	50	100	50	100	μA
		—	10	100	—	100	—	
		—	15	500	—	500	—	
Output Voltage: Low-Level, V _{OL} High-Level, V _{OH}		—	5-10	0.01	0.01	0.01	0.01	V
		—	5	4.49	4.49	4.49	4.49	
		—	10	9.99	—	9.99	—	
Noise Margin: V _{NML} V _{NMH}	Any Input	0.5 1	5 10	1 1.5	1 —	1 1.5	1 —	V
	Any Input	4.5 9	5 10	1 1.5	1 —	1 1.5	1 —	
Output Drive Current: N-Channel (Sink), I _{DN} (min.) P-Channel (Source), I _{DP} (min.)	Any Output	0.4 0.5	5 10	1.6 3.6	1.6 —	1.6 3.6	1.6 —	mA
	Any Output	4.6 9.5	5 10	-1.6 -3.6	-1.6 —	-1.6 -3.6	-1.6 —	
Data Output Off-Resistance, R _O (Off)	CS Low	—	5-10	5	5	5	5	MΩ
Input Leakage, I _{IL} , I _{IH}	Any Input	—	5-10	±1	±1	±1	±1	μA
Dynamic: t _r , t _f = 10 ns, C _L = 100 pF								
Propagation Delay Time: MRD or CS to DO, t _{ED}			5 10	150 75	150 —	150 75	150 —	ns
			5 10	150 75	150 —	150 75	150 —	
MRD or CS to DB, t _{EB}			5 10	100 50	100 —	100 50	100 —	ns
			5 10	100 50	100 —	100 50	100 —	
DI to DB, t _{IB}			5 10	100 50	100 —	100 50	100 —	ns
			5 10	100 50	100 —	100 50	100 —	
DB to DO, t _{BD}			5 10	100 50	100 —	100 50	100 —	ns
			5 10	100 50	100 —	100 50	100 —	

CDP1858

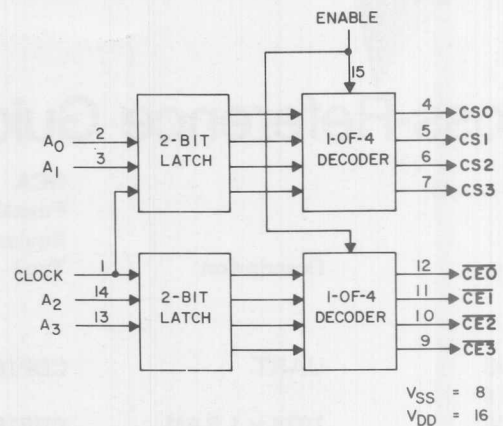
4-Bit Latch with 1 of 4 Decoder



- Designed for use with 1024 x 1 (CDP1821) organized memories
- Low power usage
- Fully static circuitry
- Single 3-12V power supply
- Enable pin allows for easy expansion above 4K bytes of memory
- Directly interfaces with CDP1802 microprocessor

CDP1859

4-Bit Latch with Dual 1 of 4 Decoders



- For use with 256 x 4 (CDP1822) memories
- Low-power CMOS
- Fully static circuitry
- Enable pin for easy expansion above 4K byte memory systems
- Directly interfaces with CDP1802 microprocessor

ELECTRICAL CHARACTERISTICS at TA = 25°C, tr = tf = 10 ns, CL = 100 pF

CHARACTERISTIC	CONDITIONS			TYPICAL VALUES				UNITS
	V _O (V)	V _{DD} (V)	CDP1858D	CDP1858CD	CDP1859D	CDP1859CD		
Static								
Quiescent Device Current, I _L (max.)		— — —	5 10 15	50 100 500	100 — —	50 100 500	100 — —	μA
Output Drive Current: N-Channel (Sink), I _{DN} (min.)		0.4 0.5	5 10	1.6 3.6	1.6 —	1.6 3.6	1.6 —	mA
P-Channel (Source), I _{DP} (min.)		4.6 9.5	5 10	-1.6 -3.6	-1.6 —	-1.6 -3.6	-1.6 —	
Dynamic:								
Propagation Delay Time: Clock _{LH} to CS0, CS1, CS2, or CS3	Enable=0		5 10	220 110	220 —	— —	— —	ns
Clock _{LH} to $\overline{\text{CE0}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, or $\overline{\text{CE3}}$	$\overline{\text{Enable}}=0$		5 10	— —	— —	220 110	220 —	ns
Clock _{LH} to A8, A9, $\overline{\text{A8}}$ or $\overline{\text{A9}}$			5 10	— —	— —	200 100	200 —	ns
$\overline{\text{Enable}}_{\text{HL}}$ to any output	Clock=1		5 10	170 85	170 —	— —	— —	ns
$\overline{\text{Enable}}_{\text{LH}}$ to any output	Clock=1		5 10	170 85	170 —	— —	— —	ns
$\overline{\text{Enable}}_{\text{HL}}$ to $\overline{\text{CE0}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, or $\overline{\text{CE3}}$	Clock=X		5 10	— —	— —	170 85	170 —	ns
$\overline{\text{Enable}}_{\text{LH}}$ to $\overline{\text{CE0}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, or $\overline{\text{CE3}}$	Clock=X		5 10	— —	— —	170 85	170 —	ns
MA0, MA1 to CS0, CS1, CS2, or CS3	Clock=1 $\overline{\text{Enable}}=0$		5 10	200 90	200 —	— —	— —	ns
MA2, MA3 to $\overline{\text{CE0}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, or $\overline{\text{CE3}}$	Clock=1 $\overline{\text{Enable}}=0$		5 10	200 90	200 —	— —	— —	ns
MA0, MA1 to A8; $\overline{\text{A9}}$, $\overline{\text{A8}}$ or $\overline{\text{A9}}$	Clock=X		5 10	— —	— —	150 75	150 —	ns
MA2, MA3 to $\overline{\text{CE0}}$, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, or $\overline{\text{CE3}}$	Clock=1 $\overline{\text{Enable}}=0$		5 10	— —	— —	200 90	200 —	ns
X = DON'T CARE								

Cross-Reference Guide

Type	Description	RCA Functionally Equivalent Type
AMI		
S1883	UART	CDP1854
S3514		
S4006	1024 x 1 RAM	CDP1821S
S4025	1024 x 1 RAM	CDP1821S
S5101	256 x 4 RAM	CDP1822S*
S6508	1024 x 1 RAM	CDP1821S
S6810-1	128 x 8 RAM	CDP1823S
S6830	1024 x 8 ROM	CDP1833/ CDP1834
Fairchild		
MK3514	512 x 8 ROM	CDP1831/ CDP1832
MK386k	I/O	CDP1852
MK35342	1024 x 1 RAM	CDP1821S
MK35345	1024 x 1 RAM	CDP1821S
MK93415	1024 x 1 RAM	CDP1821S
MK93425	1024 x 1 RAM	CDP1821S
General Instruments		
AY-5-1013	UART	CDP1854
Hughes		
HMPS1802	CPU	CDP1802*
HMPS1822	256 x 4 RAM	CDP1822*
HMPS1824	32 x 8 RAM	CDP1824*
HMPS1852	I/O Port	CDP1852*
Intel		
2704	512 x 8 PROM	CDP1831/ CDP1832*
2101	256 x 4 RAM	CDP1822S*
2308	1024 x 8 ROM	CDP1833/ CDP1834
2708	1024 x 8 PROM	CDP1833/ CDP1834*
2111	256 x 4 RAM	CDP1822S
2112	256 x 4 RAM	CDP1822S
3212	I/O	CDP1852
4101	256 x 4 RAM	CDP1822S
5101	256 x 4 RAM	CDP1822S
8101	256 x 4 RAM	CDP1822S
8212	I/O	CDP1852
8708	1024 x 8 ROM	CDP1833/ CDP1834

Note: RCA functionally equivalent type may not be identical with other manufacturer's type in every detail. Refer to manufacturer's published data for further information.

Type	Description	RCA Functionally Equivalent Type
Intersil		
IM6508	1024 x 1 RAM	CDP1821S
IM6561	256 x 4 RAM	CDP1822S
IM6402/6403	UART	CDP1854*
Mostek		
MK4006P-6	1024 x 1 RAM	CDP1821S
MK4008-9	1024 x 1 RAM	CDP1821S
MK4102P-1	1024 x 1 RAM	CDP1821S*
MK4102N-1	1024 x 1 RAM	CDP1821S*
MK2500P	512 x 8 ROM	CDP1831/ CDP1832
MK2600P	512 x 8 ROM	CDP1831/ CDP1832
Motorola		
MCM6810	128 x 8 RAM	CDP1823S
MCM6830	1024 x 8 ROM	CDP1833/ CDP1834
MCM2102	1024 x 1 RAM	CDP1821S*
National		
INSB212	I/O	CDP1852
MM74C930	1024 x 1 RAM	CDP1821S
MM87S295/6	512 x 8 EAROM	CDP1831/ CDP1832
MM2102	1024 x 1 RAM	CDP1821S*
MM5204C	512 x 8 PROM	CDP1831/ CDP1832
MM5232	512 x 8 ROM	CDP1831/ CDP1832
MM5233	512 x 8 ROM	CDP1831/ CDP1832
Texas Instruments		
TMS4039	256 x 4 RAM	CDP1822S
TMS6011	UART	CDP1854*
SN54S/74S474	512 x 8 ROM	CDP1831/ CDP1832
SN54S/74S475	512 x 8 ROM	CDP1831/ CDP1832
Western Digital		
TR1602A	UART	CDP1854*

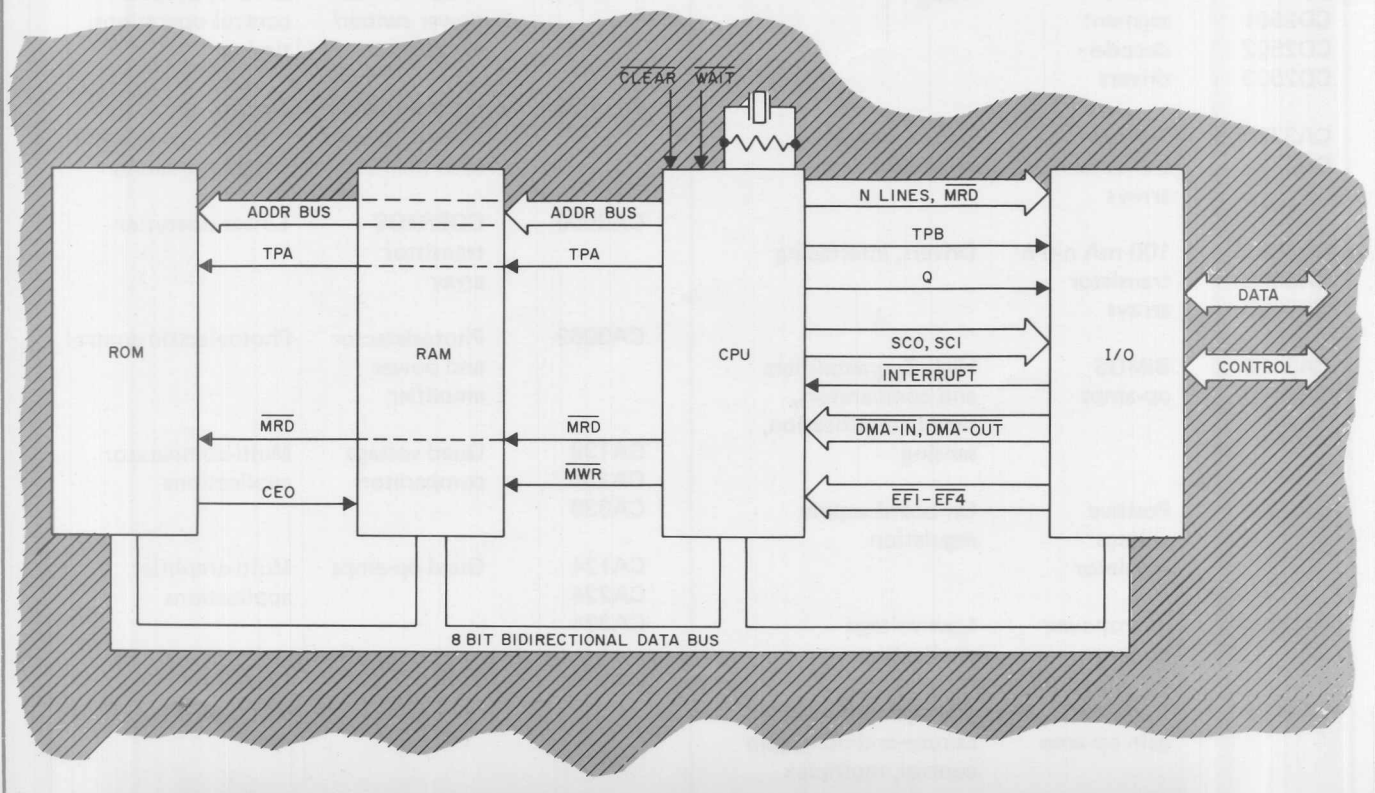
*Pin-for-pin compatible.

Interfacing and Systems Operations require support items not included in the 1800-series microprocessor product line.

Some of the items needed to interface with and control a CDP1802-based microprocessor system include:

- COS/MOS Digital Integrated Circuits
- Linear Integrated Circuits
- Clocking
- Power Supplies

Typical CDP1802 microprocessor system



COS/MOS Integrated Circuits

Circuit	Function	Application
CD4016 CD4066	Transmission gates	Interfacing non-3-state output devices to the data bus
CD4049 CD4050 CD40109	Level shifters	Interfacing components of various voltage levels
CD4041 CD4050 CD4049 CD4502	Bus drivers	Bus driving into large loading
CD4028 CD4514 CD4515 CD4555 CD4556	Decoders	Memory address or N-bit lines
CD4056 CD4511	Display devices	Interfacing data bus to display devices

Circuit	Function	Application
CD4520 CD4060	Timers/counters	External time-keeping or sequence counting
CD40105	FIFO	Interfacing systems with different clock rates
CD40101	Parity generation/decoder	Parity generation and detection
CD4034 CD4042 CD4076 CD4508	Data latches	Byte output devices
CD4014 CD4015 CD4017 CD4021 CD4034 CD4094 CD40104 CD40194	Shift registers	Serial I/O

Linear Integrated Circuits

Circuit	Function	Application
CD2500 CD2501 CD2502 CD2503	BCD-to-7-segment decoder-drivers	Display
CA3724 CA3725	1-A n-p-n transistor arrays	Relays, lamps, solenoid drivers
CA3081 CA3082 CA3083	100-mA n-p-n transistor arrays	Drivers, interfacing
CA3130 CA3140	BiMOS op-amps	High- Z_{IN} amplifiers and comparators, signal amplification, sensing
CA3085	Positive voltage regulator	On-board supply regulation
CA3078	Micropower op-amp	Low-voltage applications
CA3080	Variable-gain op-amp	Voltage comparator, sample-and-hold, gain control, multiplex

Circuit	Function	Application
CA3094	Programmable power switch/amplifier	General-purpose control operations, timing
CA3098	Programmable Schmitt trigger with memory	Control applications, time delays, Schmitt trigger switching
CA3600	COS/MOS transistor array	Linear operation
CA3062	Photodetector and power amplifier	Photoelectric control
CA139 CA239 CA339	Quad voltage comparators	Multi-comparator applications
CA124 CA224 CA324	Quad op-amps	Multi-amplifier applications
CA555	Timer	Precision timing and oscillator applications

Clocking

Clock signal generation for the CDP1802 COSMAC microprocessor is simple and straightforward. The CDP1802 features of static operation, single-phase clock, and on-chip oscillator make practical use of a low-cost, highly stable, crystal-controlled oscillator as its clock generator. The design of external oscillators for this purpose, crystal or RC controlled, is equally straightforward since they require only minimal circuitry. Recommended RC-controlled oscillator circuits include:

1. Inverter-type oscillators
2. RC oscillator using COS/MOS IC type CD4047A
3. Schmitt-trigger type RC oscillator

For reliable operation, any A-T cut crystal oscillator may be used as long as the crystal frequency is less than or equal to the maximum operating frequency specified in the CDP1802 data sheet. For improved stability, a parallel load capacitance of 20 to 24 pF is recommended.

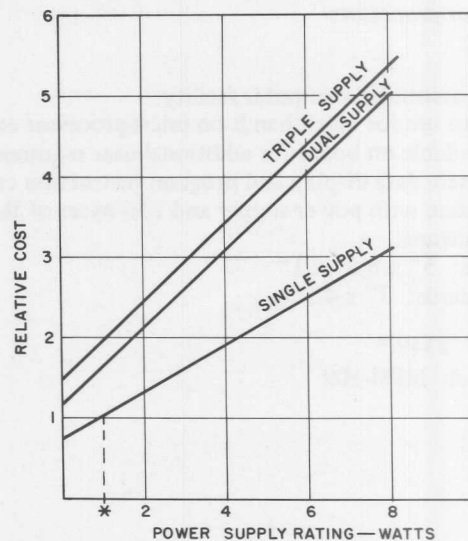
Possible crystal suppliers include:

Bliley Electronic Co.
Erie Technological Products
CTS Knights

Power Supplies

The cost of a power supply for use with the CDP1802 COSMAC microprocessor is minimized because of the advantages of the CMOS technology. The wide-operating-voltage range of 3 to 12 volts and the single power-supply requirement make CDP1802 systems design simple and straightforward.

In fact, only a CMOS microprocessor like the CDP1802 is suitable for portable and battery back-up applications. Microprocessor systems incorporating the CDP1802, CDP1832, CDP1824, and CDP1852 have a typical power dissipation of only 100 mW. These small power requirements minimize power-supply costs and help to make COSMAC systems the first and best choice.



* TYPICAL POWER SUPPLY REQUIREMENTS FOR COSMAC BASED SYSTEM.

Support Systems for the CDP1802 COSMAC microprocessor include an extensive line of hardware, software, and supplemental literature.

Features

- Full spectrum of design aids: software, hardware, support, and literature
- Low cost systems for complete system design and debugging functions
- Hardware and software application support at your fingertips
- Offers "graduated steps" to microprocessor design
- Complete series of necessary literature and application notes

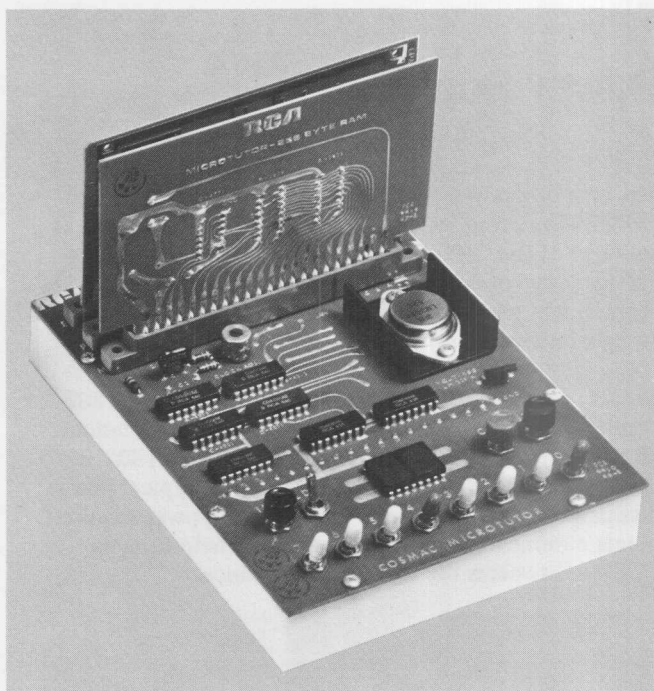
CDP18S011
CDP18S004
CDP18S800
CDP18S020
CDP18S021
CDP18S826
CDP18S91X

Microtutor
COSMAC Development System
Floppy Disk System
COSMAC Evaluation Kit
Microterminal
Fixed Point Arithmetic Package
CSDP

Microtutor CDP18S011

*To learn about programming
and microprocessors*

- Fully assembled computer facility
- Easy to use for quick hands-on microprocessor experience
- Expandable on board for additional user requirements
- Alternate data display and program instruction capability
- Complete with power supply and 256 bytes of RAM
- Dimensions:
 - Base: 5" x 6.5" x 1"
 - PC cards: 3" x 4.5"
- Price: \$349.*
- Manual: MPM-109

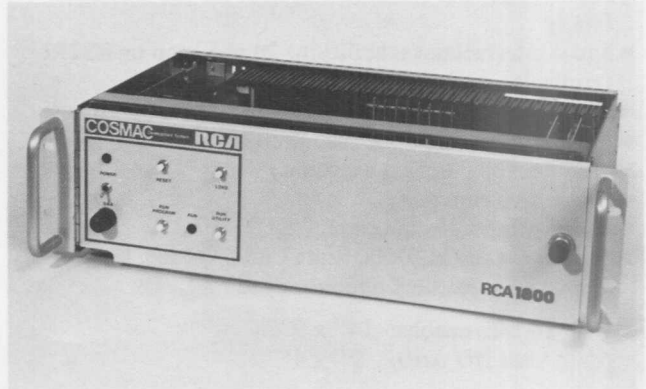


* RCA's Original Equipment Manufacturers price in the U.S.A. only.

COSMAC Development System CDP18S004

*For complete hardware and software
system development*

- Resident assembler and editor included for programming ease
- Fully assembled software development system
- Hardware testing and prototyping capability
- Complete debugging capability
- Interfaces directly to Floppy Disk (CDP18S800) and CRT, TTY (20 μ A or RS232C), or high-speed printer
- 4K RAM included (expandable to 65K)
- Over-all Dimensions: Length: 19"
Width: 11"
Height: 5.5"
Rack Mountable
- Price: \$3200.*
- Manuals: MPM-208 and MPM-201A



* RCA's Original Equipment Manufacturers price in the U.S.A. only.

Floppy Disk System CDP18S800

*For high-speed program and
data processing*

- Interfaces directly to COSMAC Development System (CDP18S004)
- Dual disk drive mechanism
- Monitor and disk control programs in firmware
- Programmed system diskette and blank diskette supplied
- 250K byte capability per diskette
- Rapid assembly, edit, and debug capability
- Disk-to-tape, disk diagnostic, memory save, assemblers, and editor, software supplied
- Additional software available
- Extra blank diskettes available (CDP18S829)
- Over-all Dimensions: Length: 19"
Width: 17"
Height: 9"
- Price: \$3320.*
- Manual: MPM-211



* RCA's Original Equipment Manufacturers price in the U.S.A. only.

Evaluation Kit
CDP18S020

Complete system for machine-language programming and prototyping

- Prototyping and evaluation system for the COSMAC family
- Serial interfacing capability to 20 mA loop or RS232 terminals
- Memory expandable on board to 4K (pre-bussed)
- Large separate area for user circuitry
- Microterminal option available
- Single-step capability
- On-board monitoring capability
- Memory Address, Data, State Code, Q-Line, Clear, Wait signals all monitored and displayed on LEDs
- Over-all Dimensions: 14" x 9.7"
User I/O Area: 7" x 4"
- Price: \$249.*
- Manuals: MPM-203 and MPM-201A

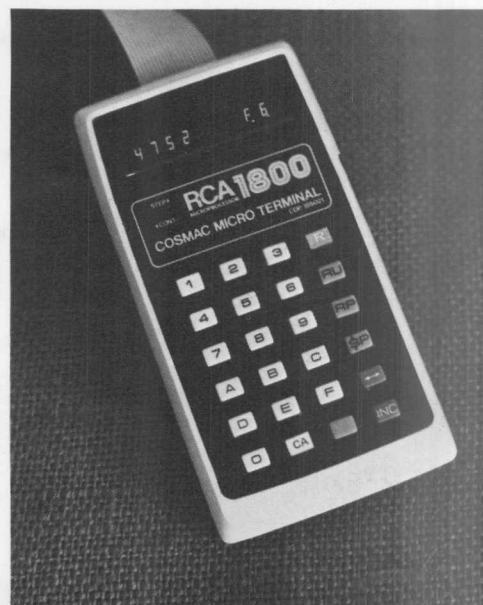


* RCA's Original Equipment Manufacturers price in the U.S.A. only.

Microterminal
CDP18S021

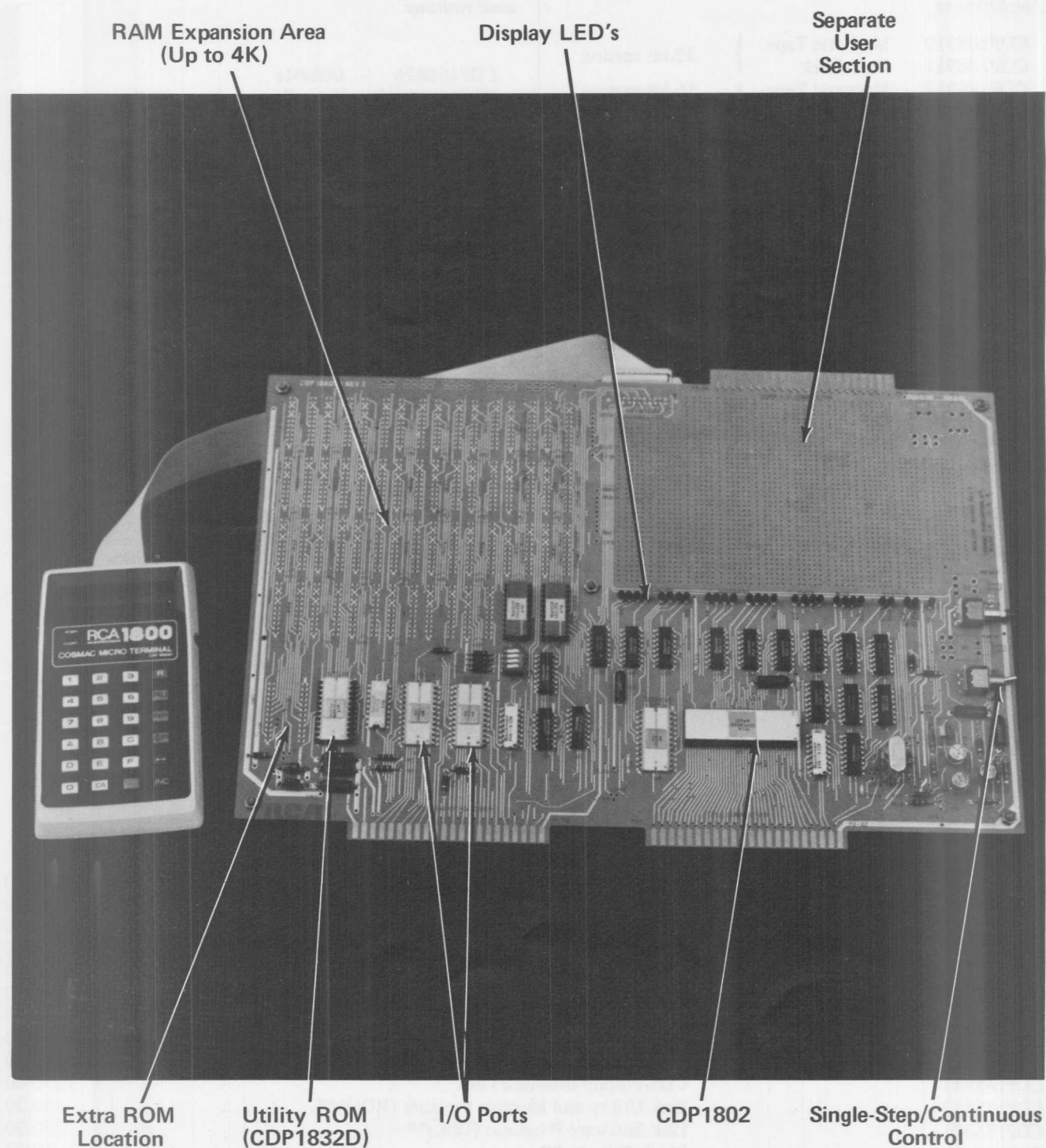
Low-cost alternative for TTY, CRT, or other intelligent terminals

- Fully assembled, portable, self-contained terminal
- Can be directly accessed as an output display
- 8-digit, 7-segment, LED hexadecimal display capability
- Features simultaneous memory address and data display
- Alternate display modes by use of CMOS utility program subroutines
- Over-all Dimensions: Length: 5.5"
Width: 3"
Height: 0.7"
- Price: \$140.*
- Manual: MPM-212



* RCA's Original Equipment Manufacturers price in the U.S.A. only.

Assembled Evaluation Kit With Microterminal



COSMAC Software Development Package (CSDP)

*For timeshare program
development*

CDP18S910	Magnetic Tape	}	32-bit version
CDP18S911	Card Deck		
CDP18S912	Magnetic Tape	}	16-bit version (HP-2100)
CDP18S913	Card Deck		
CDP18S914	Magnetic Tape	}	16-bit version (PDP-11)
CDP18S915	Card Deck		

- Cross-assembler, simulator, editor, debugger
- One-pass assembler with Level I and Level II assembly language power
- Versatile, powerful, and easy-to-use editor
- Interactive simulator/debugger acts as a "software oscilloscope" for multiple debug features
- Directly downloads programs into COSMAC Development System
- Price: \$1250.*
- Manuals: MPM-202 and MPM-204

* RCA's Original Equipment Manufacturers price in the U.S.A. only.

Binary Arithmetic Subroutine Fixed-Point Package

*To ease programming of often
used routines*

CDP18S826	Diskette
CDP18S826V1	Paper Tape
CDP18S826V2	Cassette Tape

- Consists of 31 routines including register save and mathematical companion operations
- 16-bit 2's-complement arithmetic subroutines
- Features double precision capability for the basic functions of (+), (-), (X), and (÷)
- BCD $\rightleftharpoons$ binary conversion
- All functions executed in 0.05 ms to 32 ms at 6-MHz clock rate
- Available on diskette or tape
- Price: \$100.*
- Manual: MPM-206

* RCA's Original Equipment Manufacturers price in the U.S.A. only.

*To complement your COSMAC microprocessor
system development tools*

		Price*
CDP18S200	1K RAM Card†	\$ 265.00
CDP18S201	4K RAM Card†	475.00
CDP18S202	Memory Bank Select Card†	75.00
CDP18S400	512-Byte PROM Card†	250.00
CDP18S500	Monitor Card†	500.00
CDP18S501	Byte I/O Card†	125.00
CDP18S502	Extender Card†	100.00
CDP18S504	Terminal Interface Card†	110.00
CDP18S801	Floppy Disk Drive**	3000.00
CDP18S811	CDS-Floppy Interface Card**	270.00
CDP18S812	Disk Utility and Monitor Program (ROM)**	150.00
CDP18S821	Disk Software Programs (Disk)**	250.00
CDP18S829	Blank Diskette**	10.00

† Included with CDS.

**Includes complete CDS interface.

* RCA's Original Equipment Manufacturers prices in the U.S.A. only.

Manuals

MPM-109	COSMAC Microtutor Manual	MPM-206	Binary Arithmetic Subroutines for RCA COSMAC Microprocessors
MPM-201A	User Manual for the CDP1802 COSMAC Microprocessor	MPM-208	Operation Manual for the RCA COSMAC Development System
MPM-202	Timesharing Manual for the CDP1802 COSMAC Microprocessor	MPM-211	Instruction Manual for the COSMAC Floppy Disk System
MPM-203A	Evaluation Kit Manual for the RCA-CDP1802 Microprocessor	MPM-212	Instruction Manual for the RCA COSMAC Microterminal
MPM-204	Installation Manual for the RCA COSMAC Software Development Package		

Application Notes

ICAN-6416	An Introduction to Microprocessors and the RCA COSMAC COS/MOS Microprocessor	ICAN-6491	PROM Programmer for RCA COSMAC Development Systems
ICAN-6482	Programmable Interval Timer and Counter for use with the RCA COSMAC Development Systems	ICAN-6509	Using the RCA-CDP1802 Microprocessor in CDP1801 Designs
ICAN-6485	Interrupt Priority Resolution Circuit for use with RCA COSMAC Development Systems	ICAN-6516	Hexadecimal Keyboard Interface for use in the RCA COSMAC Development Systems
ICAN-6486	Adding Two-Level I/O Interface Capability to RCA COSMAC Development Systems	ICAN-6525	Guide to Better Handling and Operation of CMOS Integrated Circuits
ICAN-6487	Hexadecimal Display for use with RCA COSMAC Development Systems	ICAN-6562	Register-Based Output Function for RCA COSMAC Microprocessors
ICAN-6488	Alphanumeric Display for use with RCA COSMAC Development Systems	ICAN-6565	Design of Clock Generators for use with RCA COSMAC Microprocessors
ICAN-6490	Analog-to-Digital Converter for use with RCA COSMAC Development Systems	ICAN-6581	Power-On Reset/Run Circuits for the RCA CDP1802 COSMAC Microprocessor

COSMAC Register and Instruction Summary

Register Summary

D	8 Bits	Data Register (Accumulator)
DF	1 Bit	Data Flag (ALU Carry)
R	16 Bits	1 of 16 Scratchpad Registers
P	4 Bits	Designates which register is Program Counter
X	4 Bits	Designates which register is Data Pointer
N	4 Bits	Holds Low-Order Instr. Digit
I	4 Bits	Holds High-Order Instr. Digit
T	8 Bits	Holds old X, P after Interrupt (X is high-order 4 bits)
IE	1 Bit	Interrupt Enable
Q	1 Bit	Output Flip-Flop

Instruction Set

The COSMAC instruction summary is given below. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)

R(W).1: Higher-order byte of R(W)

NO = Least significant Bit of N Register

Operation Notation

$M(R(N)) \rightarrow D; R(N) + 1$

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

Instruction Summary

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N))-D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))-D; R(N) + 1
LOAD VIA X	LDX	F0	M(R(X))-D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))-D; R(X) + 1
LOAD IMMEDIATE	LDI	F8	M(R(P))-D; R(P) + 1
STORE VIA N	STR	5N	D-M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D-M(R(X)); R(X) - 1
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) + 1
DECREMENT REG N	DEC	2N	R(N) - 1
INCREMENT REG X	IRX	60	R(X) + 1
GET LOW REG N	GLO	8N	R(N).0-D
PUT LOW REG N	PLO	AN	D-R(N).0
GET HIGH REG N	GHI	9N	R(N).1-D
PUT HIGH REG N	PHI	BN	D-R(N).1
LOGIC OPERATIONS**			
OR	OR	F1	M(R(X)) OR D-D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D-D; R(P) + 1
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D-D
EXCLUSIVE OR IMMEDIATE	XRI	F8	M(R(P)) XOR D-D; R(P) + 1
AND	AND	F2	M(R(X)) AND D-D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D-D; R(P) + 1
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)-DF, 0-MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76*	SHIFT D RIGHT, LSB(D)-DF, DF-MSB(D)
RING SHIFT RIGHT	RSHR	FE	SHIFT D LEFT, MSB(D)-DF, 0-LSB(D)
SHIFT LEFT	SHL		
SHIFT LEFT WITH CARRY	SHLC	7E*	SHIFT D LEFT, MSB(D)-DF, DF-LSB(D)
RING SHIFT LEFT	RSHL		

Instruction Summary (cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
ARITHMETIC OPERATIONS**			
ADD	ADD	F4	$M(R(X)) + D \rightarrow DF, D$
ADD IMMEDIATE	ADI	FC	$M(R(P)) + D \rightarrow DF, D$; $R(P) + 1$
ADD WITH CARRY	ADC	74	$M(R(X)) + D + DF \rightarrow DF, D$
ADD WITH CARRY, IMMEDIATE	ADCI	7C	$M(R(P)) + D + DF \rightarrow DF, D$; $R(P) + 1$
SUBTRACT D	SD	F5	$M(R(X)) - D \rightarrow DF, D$
SUBTRACT D IMMEDIATE	SDI	FD	$M(R(P)) - D \rightarrow DF, D$; $R(P) + 1$
SUBTRACT D WITH BORROW	SDB	75	$M(R(X)) - D - (NOT DF) \rightarrow DF, D$
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	$M(R(P)) - D - (NOT DF) \rightarrow DF, D$; $R(P) + 1$
SUBTRACT MEMORY	SM	F7	$D - M(R(X)) \rightarrow DF, D$
SUBTRACT MEMORY IMMEDIATE	SMI	FF	$D - M(R(P)) \rightarrow DF, D$; $R(P) + 1$
SUBTRACT MEMORY WITH BORROW	SMB	77	$D - M(R(X)) - (NOT DF) \rightarrow DF, D$
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	$D - M(R(P)) - (NOT DF) \rightarrow DF, D$; $R(P) + 1$
BRANCH INSTRUCTIONS—SHORT BRANCH			
SHORT BRANCH	BR	30	$M(R(P)) \rightarrow R(P).0$
NO SHORT BRANCH (SEE SKP)	NBR	38*	$R(P) + 1$
SHORT BRANCH IF D=0	BZ	32	IF D=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF DF=1	BDF	33*	IF DF=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE	3B*	IF DF=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF DF=0	BNF		
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	RQ	31	IF Q=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF1=1	B1	34	IF EF1=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF1=0	BN1	3C	IF EF1=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF2=1	B2	35	IF EF2=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF2=0	BN2	3D	IF EF2=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF3=1	B3	36	IF EF3=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF3=0	BN3	3E	IF EF3=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF4=1	B4	37	IF EF4=1, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
SHORT BRANCH IF EF4=0	BN4	3F	IF EF4=0, $M(R(P)) \rightarrow R(P).0$ ELSE $R(P) + 1$
BRANCH INSTRUCTIONS—LONG BRANCH			
LONG BRANCH	LBR	C0	$M(R(P)) \rightarrow R(P).1$ $M(R(P) + 1) \rightarrow R(P).0$
NO LONG BRANCH (SEE LSKP)	NLBR	C8*	$R(P) + 2$
LONG BRANCH IF D=0	LBZ	C2	IF D=0, $M(R(P)) \rightarrow R(P).1$ $M(R(P) + 1) \rightarrow R(P).0$ ELSE $R(P) + 2$
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, $M(R(P)) \rightarrow R(P).1$ $M(R(P) + 1) \rightarrow R(P).0$ ELSE $R(P) + 2$
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, $M(R(P)) \rightarrow R(P).1$ $M(R(P) + 1) \rightarrow R(P).0$ ELSE $R(P) + 2$
LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, $M(R(P)) \rightarrow R(P).1$ $M(R(P) + 1) \rightarrow R(P).0$ ELSE $R(P) + 2$
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, $M(R(P)) \rightarrow R(P).1$ $M(R(P) + 1) \rightarrow R(P).0$ ELSE $R(P) + 2$
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, $M(R(P)) \rightarrow R(P).1$ $M(R(P) + 1) \rightarrow R(P).0$ ELSE $R(P) + 2$

Instruction Summary (cont'd)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38*	R(P) +1
LONG SKIP (SEE NLBR)	LSKP	C8*	R(P) +2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) +2 ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N←P
SET X	SEX	EN	N←X
SET Q	SEQ	7B	1←Q
RESET Q	REQ	7A	0←Q
SAVE	SAV	78	T←M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)←T; (X,P)←M(R(2)) THEN P←X; R(2)←1
RETURN	RET	70	M(R(X))←(X,P); R(X) +1 1←IE
DISABLE*	DIS	71	M(R(X))←(X,P); R(X) +1 0←IE
INPUT-OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X) +1; N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X) +1; N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X) +1; N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X) +1; N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X) +1; N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X) +1; N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X) +1; N LINES = 7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS←D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS←D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS←D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS←D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS←D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS←D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS←D; N LINES = 7

* THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

** THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.

AFTER AN ADD INSTRUCTION:

DF = 1 DENOTES A CARRY HAS OCCURRED

DF = 0 DENOTES A CARRY HAS NOT OCCURRED

AFTER A SUBTRACT INSTRUCTION:

DF = 1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER

DF = 0 DENOTES A BORROW. D IS TWO'S COMPLEMENT THE SYNTAX—(NOT DF) DENOTES THE SUBTRACTION OF THE BORROW

An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch + 2 execute).

Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

The long-branch instructions can:

- Branch unconditionally
- Test for D=0 or D≠0
- Test for DF=0 or DF=1
- Test for Q=0 or Q=1
- Test the status (1 or 0) of the four EF flags
- Effect an unconditional no branch

If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch.

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

The short-branch instructions can:

- Branch unconditionally
- Test for D=0 or D≠0
- Test for DF=0 or DF=1
- Test for Q=0 or Q=1
- Test the status (1 or 0) of the four EF flags
- Effect an unconditional no branch

If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch with the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch.

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

They can:

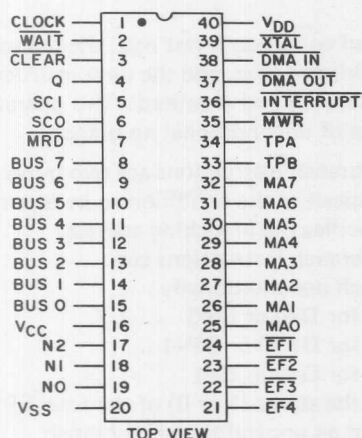
- Skip unconditionally
- Test for D=0 or D≠0
- Test for DF=0 or DF=1
- Test for Q=0 or Q=1
- Test for IE=1

If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

Terminal Assignment Diagrams

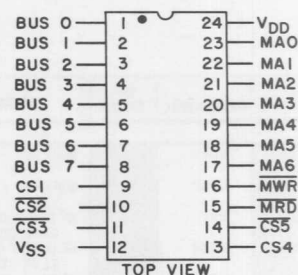
CDP1802

COSMAC
Microprocessor



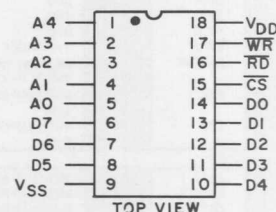
CDP1823S

124 x 8 RAM



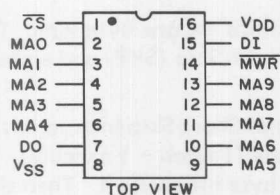
CDP1824

32 x 8 RAM



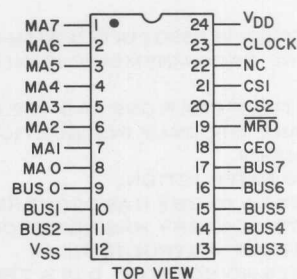
CDP1821S

1024 x 1 RAM



CDP1831

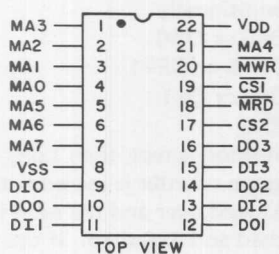
512 x 8 ROM



NC = NO CONNECTION

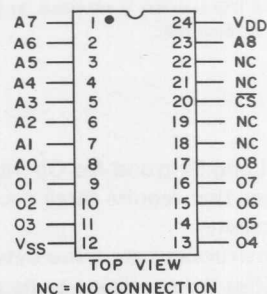
CDP1822S

256 x 4 RAM



CDP1832

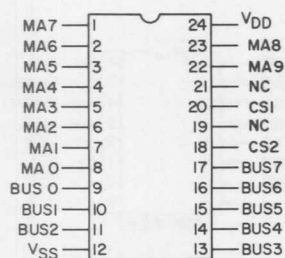
512 x 8 ROM



NC = NO CONNECTION

CDP1833

1024 x 8 ROM

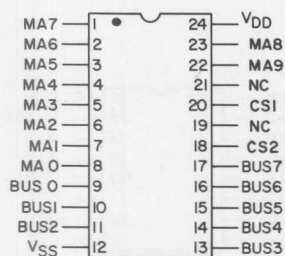


TOP VIEW

NC = NO CONNECTION

CDP1834

1024 x 8 ROM

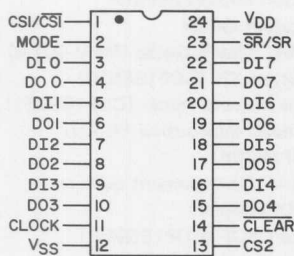


TOP VIEW

NC = NO CONNECTION

CDP1852

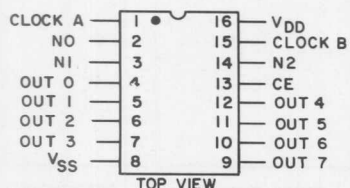
Byte I/O



TOP VIEW

CDP1853

N-Bit Decoder

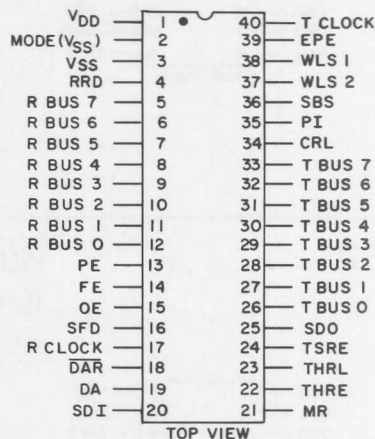


TOP VIEW

CDP1854

Mode 0

UART

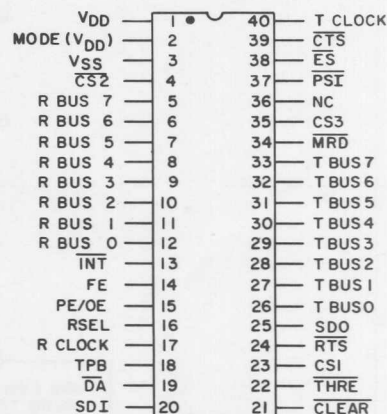


TOP VIEW

CDP1854

Mode 1

UART

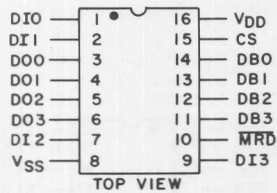


TOP VIEW

NC = NO CONNECTION

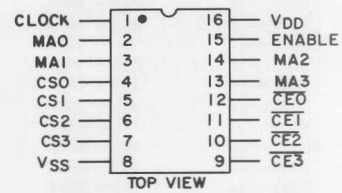
CDP1856

Bus Buffer (Memory)



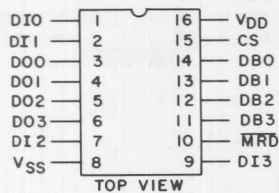
CDP1858

4-Bit Latch



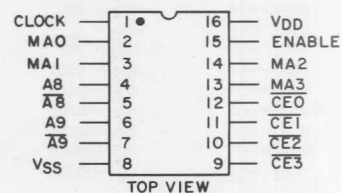
CDP1857

Bus Buffer (I/O)

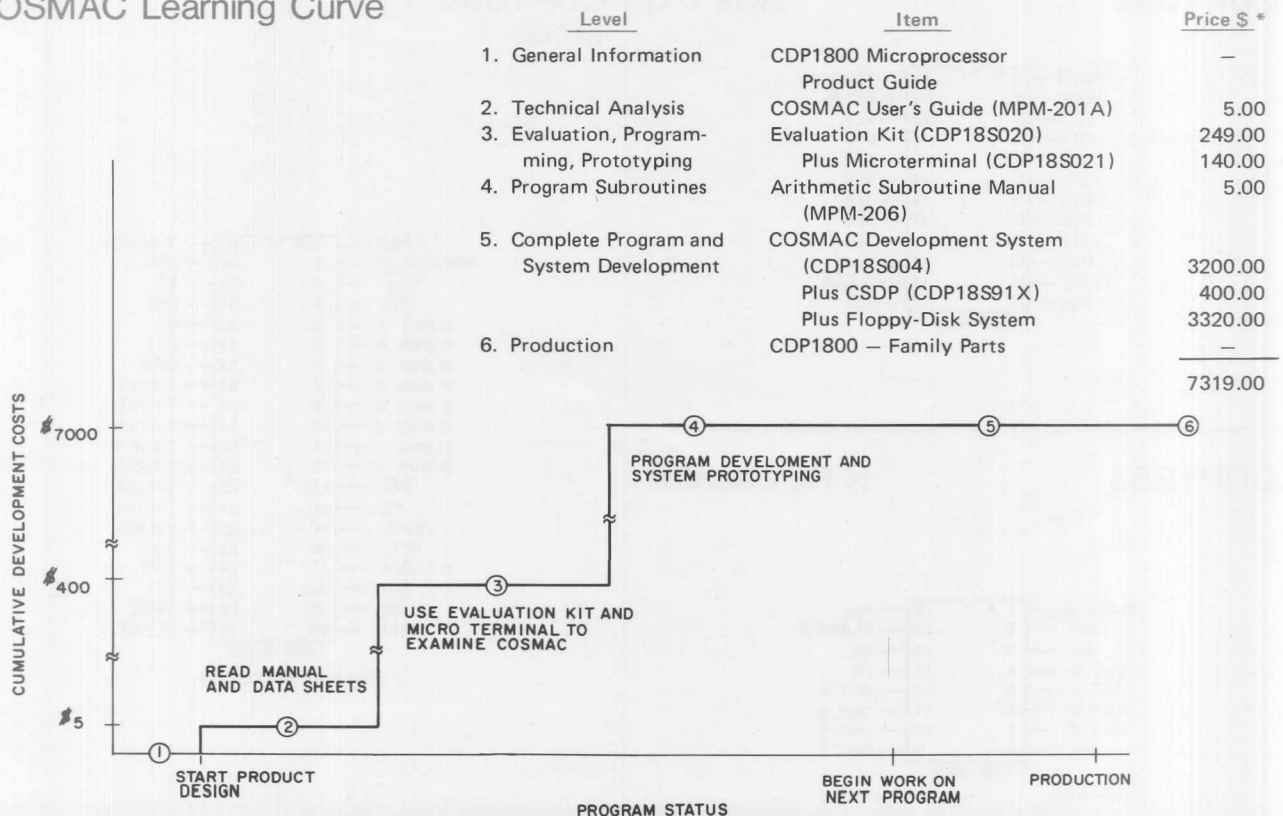


CDP1859

4-Bit Latch



COSMAC Learning Curve



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RCA Manufacturers' Representatives

Alabama	Electro-Mech , 3322 So. Memorial Pky., Suite 97, Huntsville, AL 35801	(205)883-9624
Arizona	Summit Sales , 7336 E. Shoeman Lane, Suite 104E, Scottsdale, AZ 85251	(602)994-4587
California	Bestronics (San Diego Area), 7827 Convoy Court, Suite 407, San Diego, CA 92111	(714)278-2150
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Florida	G. F. Bohman Associates , 6900 So. Orange Blossom Trail, Suite 420, Orlando, FL 32809	(305)855-0274
	G. F. Bohman Associates , 3000 N. E. 30th Place, Ft. Lauderdale, FL 33306	(305)772-9824
	G. F. Bohman Associates , PO Box 600, Clearwater, FL 33517	(813)442-5606
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Idaho	Western Technical Sales, Inc. , (No. of Boise, see Washington)	
	R² Marketing , (E. & So. of Boise, see Utah)	
Illinois	Kebco (So. Illinois Area, see Missouri)	
Indiana	Southern Sales Corporation , 3901 W. 86th Street, Indianapolis, IN 46268	(317)299-2992
Iowa	Lorenz Sales, Inc. , Suite 302, Executive Plaza, Cedar Rapids, IA 52402	(319)393-6912
Kansas	Kebco , PO Box 4806, Overland Park, KS 66204	(913)649-2168
Kentucky	Southern Sales Corporation , (see Indiana)	
Louisiana	Jackson Arnold Company , (see Texas)	
Michigan	Nicon Associates , 3835 W. Eight Mile Rd., Detroit, MI 48221	(313)341-7688
Minnesota	Comstrand, Inc. , 6279 University Avenue N.E., Minneapolis, MN 55432	(612)571-0000
Mississippi	Electro-Mech , (see Alabama and Tennessee)	
Missouri	Kebco , 11722 Studt Lane, St. Louis, MO 63141	(314)569-2660
Montana	R² Marketing , (see Utah)	
Nebraska	Lorenz Sales, Inc. , (see Iowa)	
Nevada	Summit Sales (Clark Co., see Arizona)	
New Jersey	Thomas Associates, Inc. , (So. N.J.), 304 Haddon Ave., Haddonfield, NJ 08033	(609)854-3011 (215)627-6615
New Mexico	C. T. Carlberg Associates , PO Box 3177, Station D, Albuquerque, NM 87110	(505)265-1579
New York	L-Mar Associates, Inc. , (Upstate NY) PO Box 7945, Rochester, NY 14606	(716)328-5240
	L-Mar Associates, Inc. , 216 Tilden Drive, E. Syracuse, NY 13057	(315)437-7779
North Carolina	Electro-Mech , 6700 Valley Drive, Raleigh, NC 27612	(919)782-7586
North Dakota	Comstrand, Inc. , (see Minnesota)	
Ohio	Arthur H. Baier Company , 653 Alpha Drive, Cleveland, OH 44143	(216)461-6161
	Arthur H. Baier Company , 4940 Profit Way, Dayton, OH 45414	(513)276-4128
Oregon	Western Technical Sales, Inc. , 2035 S.W. 58th Avenue, Portland, OR 97221	(503)297-1711
Pennsylvania	Arthur H. Baier Company , (W. Pa., see Ohio)	
	Thomas Associates, Inc. , (E. Pa., see New Jersey)	
South Carolina	Electro-Mech , (see Georgia and No. Carolina)	
South Dakota	Comstrand, Inc. , (see Minnesota)	
Tennessee	Electro-Mech , 1451 Elm Hill Pike, Suite 110, Nashville, TN 37210	(615)256-2516
Texas	C. T. Carlberg Associates , (El Paso Area, see New Mexico)	
	Jackson Arnold Company , (Austin, Houston, San Antonio Area), PO Box 42388, Houston, TX 77042	(713)783-7297
	Jackson Arnold Company , 1601 Lupin Lane, Austin, TX 78741	(512)447-1068
Utah	R² Marketing , 2195 So. 3600 W., Salt Lake City, UT 84115	(801)972-5646
Washington	Western Technical Sales, Inc. , PO Box 902, Bellevue, WA 98005	(206)641-3900
West Virginia	Arthur H. Baier Company , (see Ohio)	
Wisconsin	Cessop & Associates , 850 Elm Grove Road, Elk Grove, WI 53122	(414)784-3390
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Austria	Bacher Elektronische Gerate Gesmbh , Meidlinger Hauptstrasse 78, A-1120, Vienna	2462272
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Bolivia	Marconi S.R.L. , PO Box 143, Yanacocho Street 337, La Paz	
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	Cesco Electronics Ltd. , 128 Vallier West, Quebec City, Quebec	(418)524-4641
	Hamilton Avnet Int'l (Canada) Ltd. , 2670 Paulus Street, St. Laurent, Quebec H4S-1G2	(514)735-6393
	Cesco Electronics Ltd. , 24 Martin Ross Avenue, Downsview, Ontario M3J-2K9	(416)661-0220